The Impact of Interconnect Process Variations and Size Effects for Gigascale Integration

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Gerald G. Lopez

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The Impact of Interconnect Process Variations and Size Effects for Gigascale Integration

Approved by:

Professor Jeffrey A. Davis, Advisor

Professor James D. Meindl, Co-Advisor

Professor Linda S. Milor

Professor Azad J. Naeemi

Professor George F. Riley

Professor Dennis W. Hess

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For dad,

MIGUEL Lopez,

who taught me math at the age of 4 and the will to survive at the age of 30.

For mom,

Rosalinda (ROSE) Lopez,

whose tireless and unconditional love is something I can only hope to achieve.

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SUMMARY

The objective of this research is to demonstrate the impact of interconnect process variations, line-edge roughness and size effects on interconnect effective resistivity and ultimately chip performance. The investigation is accomplished through five tasks. In Task I, a new closed-form effective resistivity model, which is a function of line-edge roughness (LER), surface specularity and grain boundary reflectivity, is derived. In Task II, a critical path model is enhanced by including interconnect parasitics using the model in Task I. This enhancement also involves an extensive survey of foundry process data to shed light on the device resistance estimation used in the critical path model in Task II. Task III develops a Monte Carlo (MC) simulation framework called the Fast Interconnect Statistical Simulator (FISS). Using the latest International Technology Roadmap for Semiconductors (ITRS) projections, the FISS projects the impact of interconnect process variations and size effects onto high performance microprocessor units (HP-MPUs). Task IV fabricates metallic interconnect test structures with sub-100nm line-widths. The fifth task statistically calibrates the model from Task I using resistivity data measured from the test structures in Task IV.

CHAPTER I

INTERCONNECT SCALING

1.1 Introduction

As critical dimensions of integrated circuits shrink, the impact of process variation on the performance of these systems must be considered [1, 16–27]. In particular, the electrical performance of an integrated circuit is greatly impacted by environmental and physical factors [28]. Environmental factors that occur during chip operation include power supply variations and temperature changes across the chip. Physical factors affected during fabrication include, but are not limited to, interconnect line-width [3, 29, 30], metallic grain size [9, 10, 30, 31], and transistor channel length [8, 32–36]. While much effort has been placed on optimizing design and manufacturing at the global level for interconnects [37–47], noticeable performance degradation is occurring especially as local interconnect line-width dimensions approach the mean free path of copper (λ_{Cu}=40 nm) [1, 48]. Overall, these factors can have a great impact on the behavior exhibited by the circuit [49]. In this chapter, the primary background for this research is presented. First, the International Technology Roadmap for Semiconductors (ITRS) will be introduced and compared to industry data. Second, the sources of interconnect variation are identified. Third, a widely accepted resistivity model is reviewed and an exhaustive discussion follows describing the problem as the interconnect line-width becomes closer to λ_{Cu}. Finally, a discussion of current work related to the maximum critical path delay of MPUs closes this chapter.

1.2 Background and Motivation

The task of scaling critical dimensions requires a parallel effort to control and/or tolerate process variations because they can significantly impact the overall chip performance, power, yield and cost [1]. Of primary interest is the phenomenon of increasing wire delay from the scaling Cu interconnect [2, 3, 9, 10, 14, 15, 30, 31, 48, 50–71]. As technology continues to

scale well into the sub-100 nm regime, size effects play a significant role in interconnect performance [2, 3, 9, 10, 14, 15, 30, 31, 48, 51–54, 56, 57, 59–66, 68–72]. Noticeable performance degradation is occurring especially as the line-width dimensions approach the mean free path of copper (λ_{Cu}=40 nm). Moreover, variations in the line-width and line-height become increasingly difficult to control.

The objective of this work is to identify the key sources of interconnect variations and to model their effects on wire performance beyond the 22nm node. A major challenge of this work is determining the interaction between size effects and interconnect process variations. By modeling the interaction, insight for future technologies can be obtained using computationally fast and statistically accurate circuit-level analyses of high performance microprocessor unit (MPU) architectures. The details of such analyses will involve the derivation of a new closed-form model for interconnect resistivity as a function of line-edge roughness (LER), grain boundary reflectivity and sidewall specularity. In addition, a Monte Carlo simulation framework will use said model to predict future MPU architecture performance using a maximum critical path delay scheme. Finally, the new resistivity model will be verified using empirical resistivity measurements from wires with varying line-width.

1.2.1 Interconnect Targets: The ITRS and Industry

The International Roadmap for Semiconductors is an enumerated list of targets, organized by chapter and assembled as a collaborative effort by members within semiconductor industry. Careful use of the words *target* and *projection* is applied in this section. *Target* implies a simple goal or value for which to aspire. *Projection* implies the ability to predict a particular goal or value. Essentially, the ITRS is a wishlist for the semiconductor industry with evolving targets. In particular, there are copper interconnect targets made for high performance microprocessors (MPUs) on which this work centers. Technology nodes or generations are given in terms of their year or critical dimension (CD). The year indicates the time at which the CD will be used for mass production. The CD is defined as width the first metal layer (M1) DRAM half-pitch as illustrated in Figure 1. To clarify, a wire-pitch is the lateral spacing given for the width of the wire and the spacing needed between itself and its

neighboring wire on one side. A wire-pitch may also be referred to as the center-to-center spacing between adjacent wires. Since 2008, the DRAM half-pitch and MPU half-pitch have converged to the same target values. Therefore, assuming the M1 wire width and spacing are 1-to-1, the M1 half-pitch for every technology node is simply the width of an M1 wire for both a DRAM and/or MPU. The shrinking of the interconnect and the transistor is commonly referred to as scaling. The physical dimensions (width and height) of the interconnect scale by a factor of 0.7. In other words, every successive technology generation is 70% the physical size of the previous generation.

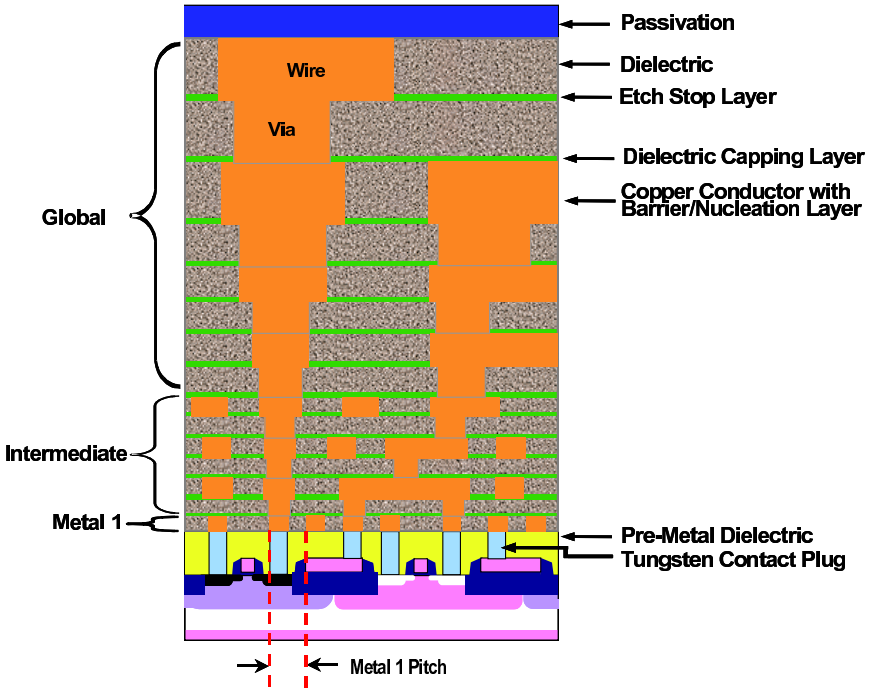

Figure 1: Copper interconnect stack as illustrated from [1].

While these targets are not *hard and fast* numbers, the goal is to help guide industry as it scales well into the 11nm node by the year 2022. In Table 1, seven technology nodes are presented comparing M1 physical line dimensions noted in the ITRS [1, 73–76] and compared to data published by Intel [77–82]. Since 22nm has yet to be achieved by Intel, *projected* dimensions have been produced for comparison using 32nm data and the scaling factor of 0.7. Noticeably, the roadmap projections are much more aggressive. In fact, since 2007 the cross-sectional area of the M1 Intel interconnects are more than twice than ITRS

Table 1: Comparison of ITRS M1 Physical Line Dimensions Targets to Intel Data

Technology Node		**Width [nm]**		**Height [nm]**		**Cross-Sectional Area Ratio: Intel/ITRS**
Year	$\frac{1}{2}$-Pitch [nm]	ITRS	Intel	ITRS	Intel	
1999	180	230	253	322	480	1.6
2001	130	150	175	240	280	1.4
2004	90	107	107	182	150	0.8
2007	65	68	106	116	170	2.3
2010	45	45	80	81	144	3.2
2013	32	32	56	61	95	2.7
2016	22	22	39*	44	67*	2.7*

*Intel projection using a scaling factor of 0.7 and 32nm dimensions.

projections. A simple explanation of this discrepancy between the ITRS and industry is the loose definition of a technology node. According to [83], the technology node once was a measure of the printed gate length of the transistor. Today, to be at any given technology node is to meet a set of criteria described by the ITRS for the transistor (i.e., transistor drive current, transistor leakage current and power envelope).

1.2.2 Size Effects and Temperature Independence

As stated earlier, noticeable performance degradation is occurring especially as the line-width dimensions approach the mean free path of copper (λ_{Cu}=40 nm). The root cause of the degradation are size effects. A size effect can be defined as a physical obstacle that exists regardless of external environmental factors such as temperature. As the interconnect continues to scale well below the λ_{Cu}, interaction of the electron with the sidewalls and grain boundaries of the interconnect becomes more pronounced. Even though the overall effective resistivity can be lowered by decreasing the temperature of a wire, size effects still increase the effective resistivity as the physical dimensions of the wire approach the λ_{Cu} (Figure 2). While the advantage to chip cooling to effective resistivity with size effects are evident, the investment to chip cooling is limited to air cooling to reduce cost. The modeling and impact of size effects will be described in greater detail later in this chapter.

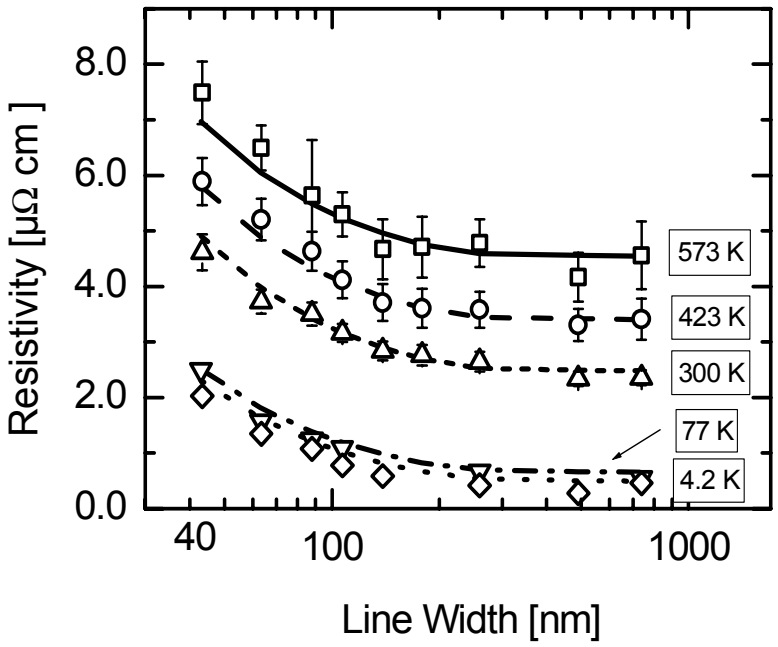

Figure 2: The impact of size effects and temperature on increasing effective resistivity [2]. Even though the overall effective resistivity can be lowered by decreasing the temperature of a wire, size effects still increase the effective resistivity as the physical dimensions of the wire approach the λ_{Cu}.

1.2.3 Process Variations

Physically, interconnects are layers of patterned metal atop or within a dielectric, which is typically an oxide as seen in Figure 3. Temperature, lateral dimensions and vertical dimension impact the electrical property of a metal line. Lateral dimensions imply the x- and y-component of dimension of a wire (Figure 3), which can be length or width depending on one's orientation. Vertical dimension refers directly to the thickness or height of the interconnect as seen in Figure 3 along the z-axis. At the electrical level, grain boundary structures and interconnect sidewalls that serve as copper diffusion barriers have been shown to vary from one process to another [3, 15, 30, 52, 56, 57, 60] and will be explained in greater detail later in this chapter. Since the metallic grain sizes and interconnect sidewalls are physically constrained by the dimensions of the interconnect [9, 10], electrical variability arises from physical variability seen along the length of the metallic wire.

Parametric variation is a term used to describe the effects of fabrication variation [84] and is organized into two groups: die-to-die (D2D) and within-die (WID). For the purposes

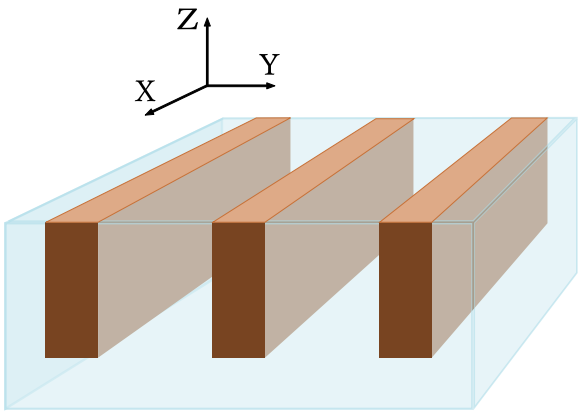

Figure 3: Orientation of the copper interconnect in oxide.

of this work, parametric variation will be used to describe the physical variations resulting from fabrication as seen in Figure 4 as they directly impact the electrical performance of the interconnect. D2D variations arising from lot-to-lot, wafer-to-wafer and some from within-wafer variations [85] come from process fluctuations in temperature [49], chemical mechanical polishing (CMP) [68] and wafer placement. Bowman [85] notes that within-wafer variations contribute to both D2D and WID fluctuations. For example, resist thickness across a wafer is random from wafer to wafer, but is deterministic within a wafer. As a result, thickness variation is deterministic across the wafer; however, when comparing resist thickness of a die from the center of the wafer to a die from the edge of the same wafer, resist thickness differs. Looking WID, resist thickness varies from one edge of the chip to the other, but varies little in thickness when examining a local area within the die.

There are two kinds of WID variation: systematic (WID-S) and random (WID-R). Smooth variations are referred to as systematic WID variations. For instance, stepper lens aberrations in lithography create a smooth nonlinear pattern variation in printed line-widths across the die, while the imperfections in the mechanics of the steppers create deviations in the pattern from die to die. Random variations, like dopant atom placement in a device channel, are referred to as random WID variations. Some WID variations can have *both* a systematic and random component. Duvall [84] explains how process conditions can vary at random from die to die, but vary deterministically within-die.

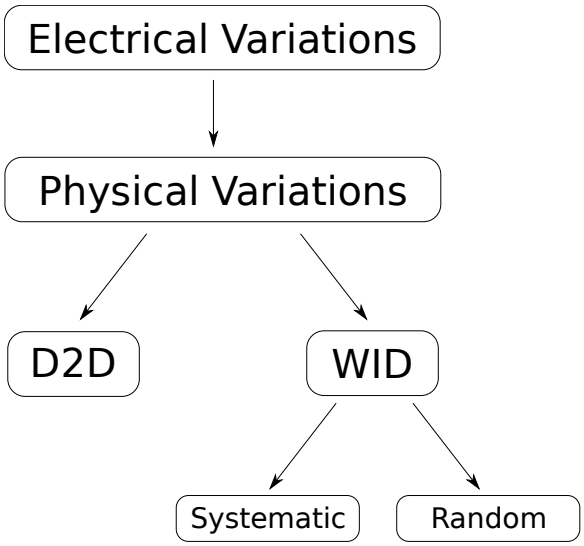

Figure 4: Hierarchy of variation for interconnects

1.3 Sources of Interconnect Process Variations

The sources of electrical variability within a design are of primary concern to a semiconductor company when fabricating a high-end microprocessor. Ultimately, these sources of variation affect the overall yield and cost of an integrated circuit. In this section, some of the main steps in chip fabrication that contribute to variability are discussed. They are photolithography, metalization, rapid thermal process (RTP) and chemical mechanical polishing (CMP). These are all used in a copper damascene process [86]. For instance, creating damascene copper interconnects begins with photolithography. Once a pattern is transferred to the resist, the resist is used as a mask so trenches can be etched into the oxide layer below. The resist is then cleared, and metalization is performed by depositing a thin barrier layer of TaN prior to the Cu deposition. To encourage reflow and grain enlargement, the wafer undergoes RTP. Finally, CMP polishes away the overburden, completing the damascene process.

1.3.1 Photolithography

Interconnects are simply patterned metal within a dielectric. The pattern is generated using photolithography. Since 2008, M1 and intermediate wiring levels (i.e., long local wires) share the same line-widths, aspect ratios, and barrier/cladding thicknesses [1]. This

implies that the variability seen at M1 will also be seen at intermediate wiring levels. To elucidate this point, interconnect critical dimension (CD) variation (M1 to intermediate level line-widths) is affected by photolithography. Stepper lens lithography contributes to both D2D and WID variations. Particularly, optical proximity correction has been used in industry to compensate for optical diffraction distortion of wire features on-chip [87]. Consequently, stepper lens aberrations create a systematic nonlinear pattern variation in printed line-widths across the die, while the imperfections in the mechanics of the steppers create deviations in the pattern from die-to-die [84].

Effective line-widths (w_0) are projected to exhibit a $\pm 3\sigma_{w_0} 10\%$ total CD variation for M1 to intermediate metal levels for all generations [76], where CD is the ITRS Microprocessor Unit (MPU) half-pitch. Aside from w_0 variation, at the physical level, fabricated interconnect lines are not perfectly straight with clean line-edges. The roughness seen along the length of wire or line-edge roughness (LER) compound the degrading performance of the interconnect. Recent studies on the impact of LER have been conducted [3, 88]. In [3], the impact of line edge roughness (LER) on ρ_{eff} is modeled as out-of-phase sinusoids. These authors use numerical simulation to predict the impact that LER can have on the effective resistivity. In addition, metrology was performed on wires generated with photolithography. It revealed that wires with w_0=40 nm can have LER variations as great as 15 nm, resulting in widths from 25 nm to 55 nm along the length of a wire [3] (see Figure 5a). Improving the photolithography technology from i-line to deep UV showed a reduction in LER, where Figure 5b illustrates an effective line-width of 60nm with an LER of 6nm. A similar value of 6nm LER can also be found in more recent work [89].

The authors in [3] showed that LER contributes greatly to wire resistivity especially if the width variation is equal or greater than 50% of the line-width [3]. Although no closed-form model was produced, it was determined that LER may no longer be neglected for line-widths below 50nm with LER amplitude exceeding 15nm. The amount of LER depends on the photolithographic and resist technology used [3, 90]. As a result, LER is assumed to be an inherent and fixed-constant by-product that is superimposed on the metal line-width, which makes it width independent.

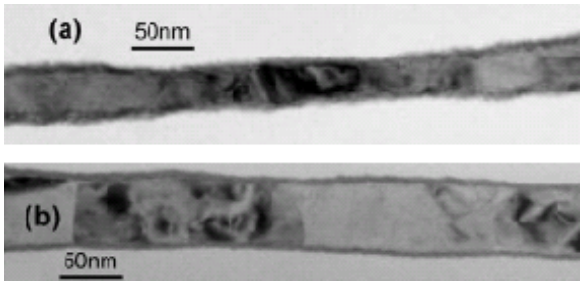

Figure 5: TEM micrographs of copper damascene interconnects from [3]. (a) Average line-width 40nm with 15nm LER. (b) Average line-width 60 nm with 6nm.

1.3.2 Metalization

Metalization is wrought with processing challenges. The most common form of Cu metalization is electrochemical plating (ECP). Other forms include filament evaporation, e-beam evaporation and sputter deposition. To prevent Cu diffusion into the surrounding oxide, a TiN, TaN and/or Ta barrier layer is applied prior to ECP. Because the barrier layer is electrically conductive, [1] considers an effective resistivity for Cu interconnects. In [63], the authors explain how the Ta crystal orientation impacts the effective resistivity. Through careful processing, the resistivity of the barrier layer can be reduced, improving electrical conduction. In [91], 20nm damascene Cu lines were fabricated and electrically tested. This work compares the challenges of barrier layer application via physical vapor deposition (PVD) and atomic layer deposition (ALD). Process challenges included partial filling and pinching. The authors also attributed variability in electrical measurement to a large variation grain structure [91]. While much work has been done in barrier deposition, others are trying to increase grain size. In [54], a novel plating chemistry is used to enlarge grain size to minimize the impact of grain boundary scattering. In [31], physical metrology indicate grain growth is influenced by the barrier layer. In fact, this work extends [63] by revealing the impact of the barrier layer to Cu grain formation. In summary, metalization presents a variety of processing challenges. Without careful processing, variations in barrier layer deposition and grain structure can have a profound impact on the effective resistivity of the copper interconnect.

1.3.3 Rapid Thermal Process

A widely used type of annealing is called rapid thermal process (RTP). Annealing originally was the process to repair the damaged silicon lattice caused by ion implantation by heating the wafer between 800°C and 1000°C [92]. Today, RTP describes a family of single-wafer hot processes that have been developed to minimize the thermal budget of a process by reducing the time at temperature in addition to, or instead of, reducing the temperature [86]. RTP provides good uniformity and reproducibility. As a result, RTP impacts wafer-to-wafer variation; however, heating and cooling the wafer uniformly to prevent warping, maintaining a uniform temperature during the process and measuring the wafer temperature are challenges still faced by process engineers [86]. RTP is attractive for producing larger metallic grains in copper interconnects to reduce resistivity [93, 94]. This process is also referred to as rapid thermal annealing (RTA). However, as interconnects are fabricated with line-widths near the mean free path of an electron in Cu, the line-width imposes a limit on the effectiveness of RTP on grain size growth [93–96]. Due to physical limitations, variation in grain structure can be expected. In short, the lateral wire dimensions at the nanometer regime play an important role in affecting the effective resistivity of an interconnect.

1.3.4 Chemical Mechanical Polishing

Chemical mechanical polishing (CMP) is a unit process that contributes to height variation for on-chip interconnects. Extensive work has been done on CMP [68], which is a known contributor to resistivity variability [97]. Studies show that the removal rate is higher at the wafer edges than at the center and that over-polishing is needed for complete copper removal [98]. Consequently, because copper metal is relatively softer than silicon oxide, metal dishing can occur. Metal dishing is defined as the recessed height of a copper line compared to the neighboring oxide [97]. Wider global wires typically experience more dishing than narrower local wires. This phenomenon is also exacerbated by the pattern density that also contributes to oxide erosion [97–99]. Oxide erosion is known as the difference between the original oxide height and the post-polish oxide height [97]. It also has been shown that over design can occur if pattern density is not considered in an ASIC design flow [40].

Lakshminarayanan et al. [61] show the effects of the underlying metal layers on the resistance of a wire created from a Damascene copper CMP process. Their research shows how a wire over an area with no underlying metal can have a higher resistance consequence of the upper metal layer conforming to that of its underlying layer. In short, wire resistance turns out to be a function of the underlying density, exhibiting a near linear dependence of the Metal 2 layer on the Metal 1 layer [61]. Considering a long wire across a chip, the underlying layer will induce a variation in resistance in addition to any dishing or erosion that may occur. Consequently, the underlying metal layers exhibiting dishing and erosion further contribute to height variability [61].

Another generally overlooked component of CMP is the thermal contribution to the removal rate of copper and slurry chemistry [100]. Sorooshian et al. [100] report that studies show that increasing the polishing temperature increases the removal rate of copper, exacerbating dishing and erosion. It has been demonstrated that the impact of pad temperature can be quantified into a single defined value in terms of activation energy [100]. If the thermal gradient across a wafer is not kept uniform, removal rates during CMP could be considerably different across the wafer than when pattern density alone is considered.

To overcome the effects of CMP, early steps were taken by examining different pattern densities [97–99], optimizing the CMP process by reducing the chemical effect [101] and creating a completely abrasive-free process (AFP) [102, 103]. However, because of the underlying metal layers, extending metal layout rules for improved manufacturability and placing the responsibility of dishing and erosion on the designer rather than on the process engineer have been proposed [61]. In addition, careful attention should be paid to the thermal contributions of pad temperature [100].

According to [1], dishing is expected to recess no more than 10% of the nominal conductor height h_0. A recent study used simulations where height variation was $\pm 3\sigma_{h_0} 10\%$ [30]. This assumption is based on the authors' metrology. In [104], results show that both dry-etching of the low-k layer and CMP intensify LER and wedges. In modeling the electrical performance of a copper interconnect with process variations from an optimized CMP process, pattern density, the effects of underlying metal density, and the resulting physical

dimensions effects on resistivity must be considered.

1.4 Interconnect Resistivity Model

A widely accepted interconnect resistivity model can be found in [2] and in its high-level form is given by

$$\rho_{eff} = \rho_0 \left(GB_{scat} + SW_{scat}\right). \tag{1}$$

This model in (1), which gives the effective resistivity (ρ_{eff}), is the product of the bulk resistivity (ρ_0) and the summation of two expressions that describe electron grain boundary reflectivity (GB_{scat}) and electron sidewall specularity (or sidewall scattering), SW_{scat}. GB_{scat} and SW_{scat} are commonly referred to as size effects. The summation of these two expressions is justified by using Matthiessen's Rule [2]. Essentially, the model starts with ρ_0 and increases ρ_0 depending on the impact from GB_{scat} and SW_{scat}. If there are no size effects, ρ_{eff} appropriately collapses to ρ_0. Unlike bulk resistivity, experimental results from [48] indicate that size effect terms are independent of temperature. With respect to temperature, the resistivity from background scattering is typical of bulk data. Background scattering as discussed in [105] arises from point defects and phonons [51].

1.4.1 Bulk Resistivity and Mean Free Path

Before explaining the salient features of each scattering model, ρ_0 and λ must be considered as their values are used to project the performance of future technology nodes [3, 53]. The value of λ which is the mean free path of an electron, is connected to the value of ρ_0. As the temperature of the conducting material is lowered, λ increases while ρ_0 decreases. Likewise, when the temperature is raised, λ decreases while ρ_0 increases. While the individual parameters λ and ρ_0 are temperature dependent, the product of λ and ρ_0 is considered a temperature independent constant. The product is, however, a function of the electron density in a given metal [4]. Although Cu has ρ_{0Cu}=1.68$\mu\Omega$-cm, there is an increase in the resistivity due to the added effect of the barrier liner, which is needed to aid in the adhesion and prevent the contamination of Cu into the surrounding dielectric. A typical barrier liner is a TaN/Ta thin film [63], and it has been shown to increase the ρ_{0Cu} [63]. As a result,

ρ_{0Cu} is considered an effective ρ_0 and as such a fit parameter, while maintaining constant the resistivity and the mean free path (λ) product [66]. In other words, the bulk resistivity and mean free path are still temperature-dependent parameters. As temperature decreases, so does ρ_0 with an increase in λ. As temperature increases, ρ_0 increases while λ decreases. Nonetheless, the product of ρ_0 and λ remains constant.

The ρ_0 of Cu/barrier and Al is 2.2 $\mu\Omega$-cm and 2.65 $\mu\Omega$-cm, respectively [1, 4]. The λ can be described as the average distance traveled by an electron between subsequent scattering events. Typical bulk values at 300K for Cu and Al are λ_{Cu}=40 nm and λ_{Al}=14 nm, respectively. These values are calculated using:

$$\lambda = v_f \tau, \tag{2}$$

where v_f is the electron speed of a material (Fermi velocity) and τ is the relaxation time of the electron of a material at a specific temperature [4]. As shown in (2), calculating λ does not require information regarding grain structure or size.

1.4.2 Scattering Models and Parameters

The sidewall scattering model in (1) is the Fuchs-Sondheimer (FS) model [106] published in 1951. Both Fuchs and Sondheimer considered the quantum effect of free electrons with a distribution of λ in bulk and also assumed that the surface of a thin film impacts the distribution of λ. The specularity parameter p found in the FS model describes SW_{scat}. The value of p can be between 0 and 1, where a value of 0 indicates that scattering is totally diffuse (inelastic), with the electrons experiencing complete loss of their drift velocity. The value p=1 indicates that all collisions are completely elastic thereby not impacting the electron drift velocity. In other words, p indicates the percentage of electrons that are to be scattered elastically at the surface of the thin film.

The grain-boundary (GB) scattering model is the Mayadas-Shatzkes (MS) model published in 1970 [105]. The MS-model assumes that GBs are partially reflecting planes perpendicular to the electric field that are a certain distance (often the grain size) apart. The MS model contains the scattering parameter R, which indicates the percentage of electrons that are scattered at the grain boundary and has a value between 0 and 1. This is to

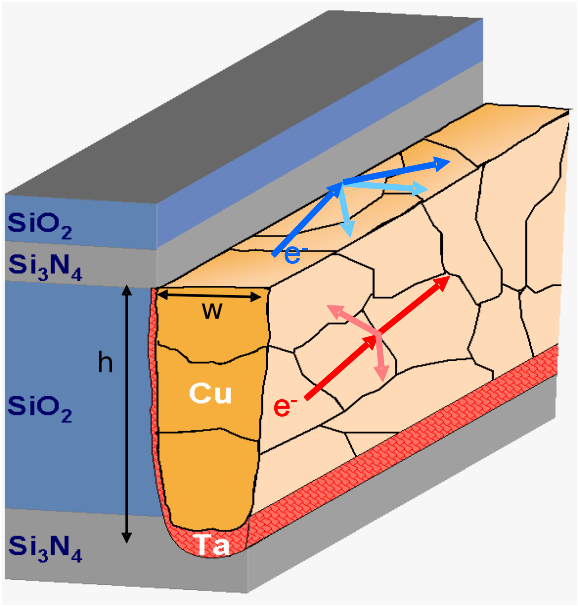

Figure 6: Detailed illustration of sidewall and grain boundary scattering in a Cu interconnect with a Ta barrier layer. Sidewall scattering is illustrated using blue arrows. Grain boundary scattering is illustrated using red arrows. The Cu interconnect thickness and width are **h** and **w**, respectively.

say that for R=1, an electron is experiencing complete internal reflection within a metallic grain. Using both parameters p and R as fit parameters to a set of resistivity vs. line-width measurements, a description of the average scattering of electrons from the sidewall and grain boundary can be extrapolated, respectively. Figure 6 illustrates the two scattering events at their respective sites. Ideally, diffuse scattering is desired at the grain boundaries (R=0) with fully elastic scattering along the sidewall of the interconnect (p=1). However, as shown in Table 2, values for the scattering parameters for Cu vary and are far from this ideal.

Table 2: A Survey of p and R Values for Cu in Published Work

Cited Work	p	R
Kitada et al. [30]	0	0.43
Chen et al. [52]	0.1	0.2
Shimada et al. [56]	0	0.5
Steinhoegl et al. [3]	0.4	0.5
Steinhoegl et al. [15]	0.25	0.13
Guillaumond et al. [60]	0.43	0.2
Besling et al. [57]	0.5	0.3

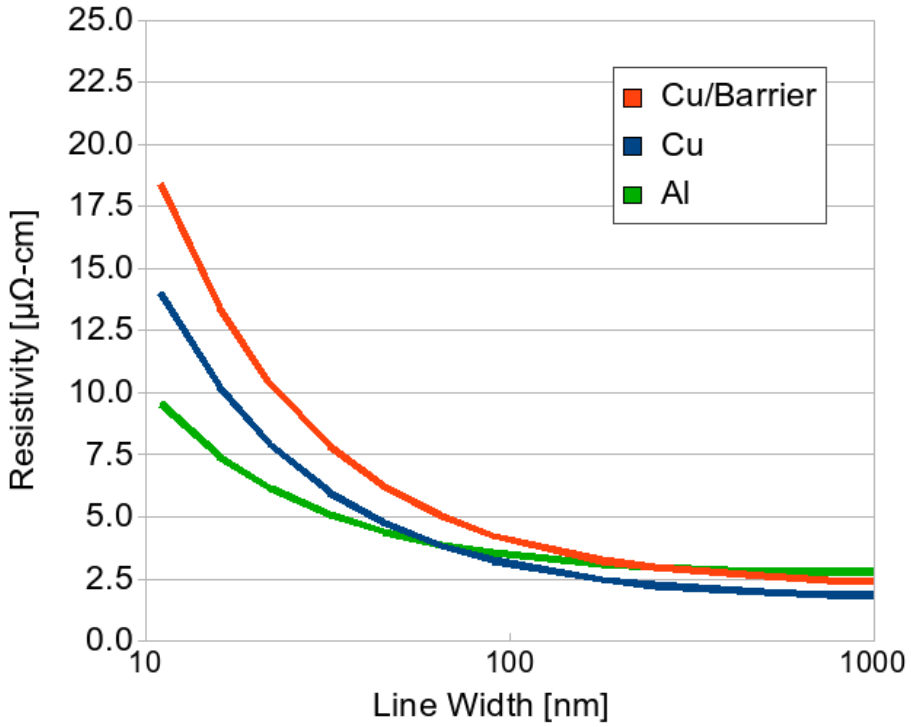

Figure 7: Graph of (1) for copper, copper/barrier, and aluminum with λ_{Cu}=40 nm, $\lambda_{Cu,Barrier}$=40nm and λ_{Al}=14 nm. The ρ_0 values of Cu, Cu/Barrier and Al is 1.7 $\mu\Omega$-cm, 2.2 $\mu\Omega$-cm and 2.65 $\mu\Omega$-cm, respectively [1, 4]. Scattering parameters are p=0 and R=0.5 for all curves.

1.4.3 Electron Mean Free Path and Scattering

So far, the discussion has established that two primary temperature-independent scattering events impede the conduction of an electron: SW_{scat} and GB_{scat}. Moreover, the product of ρ_0 and corresponding λ is approximately temperature independent. In this section, the impact of size effects as physical dimensions of a polycrystalline structure near λ is discussed. For materials with long mean free paths λ_{long} like Cu (λ_{Cu}=40nm), the λ is distorted significantly by size effects. In fact, a noticeable reduction between 38-52% is calculated for λ_{Cu} by [107], whereas a reduction in λ_{Al} is 15%, supporting that λ_{Al} is affected little by decreasing polycrystalline film thickness. Assuming scattering parameters are the same for each material, graphing the ρ_{eff} of Cu, Cu/barrier and Al reveals that Al is impacted less by the diminishing physical dimensions compared to Cu and Cu/barrier (Figure 7).

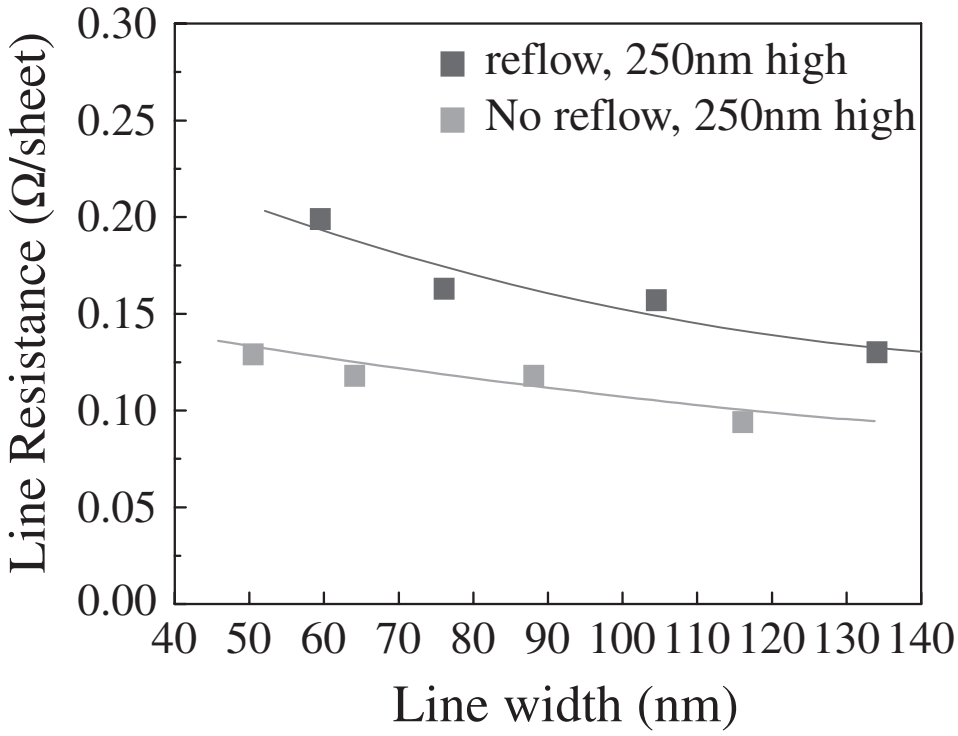

Figure 8: Line resistance vs. line-width: The impact of reflow forms $TiAl_3$ within the Al interconnect, increasing line resistance [5].

This has been shown in modeling [5, 7, 52, 53] and implies that 16nm line-width might have 50% less ρ_{eff} than copper. Increasing resistivity arises when Al is processed with a barrier liner such as Ti(N), forming $TiAl_3$ [5, 6] during reflow (Figure 8). As a result, the simulated advantages of Al vanish as shown in Figure 9 and Figure 10, where the experimentally measured ρ_{eff} of Cu and Al interconnects are compared. So while the advantages of Al may exist through modeling, realizing them are limited by process integration. An alternative barrier metal Ru may show promise to mitigate Al and barrier compounding. A simulated point of reference for Al with Ru to experimentally measured Cu $\rho_{eff}$is shown in Figure 9, however no empirical data is presented to support Al for interconnect dimensions below λ_{Cu}=40nm.

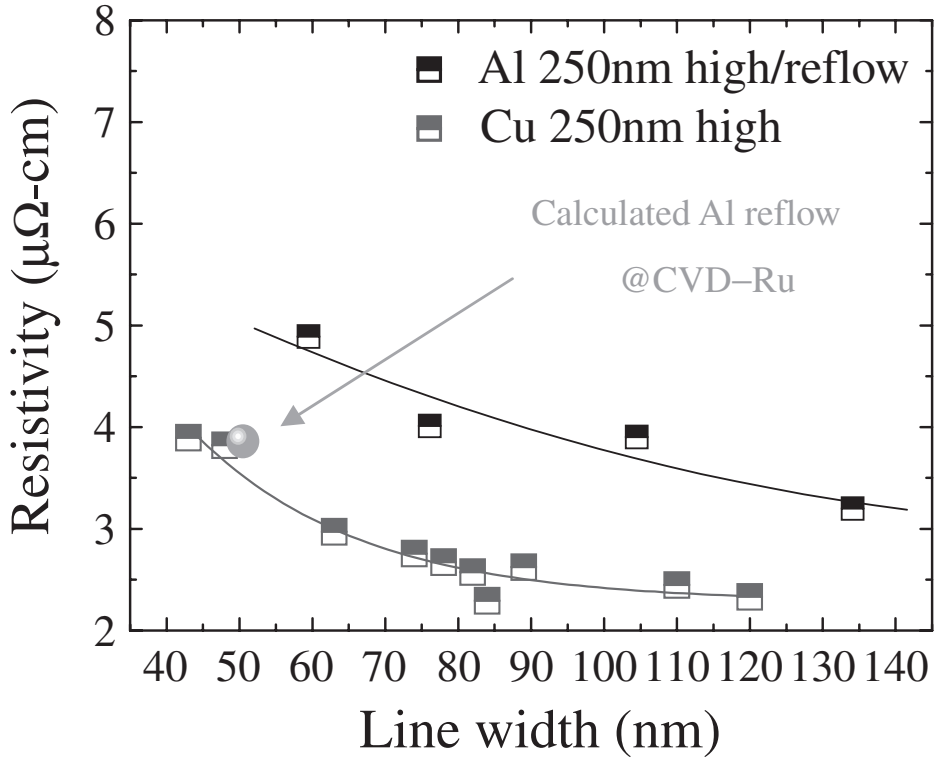

Figure 9: Al interconnect ρ_{eff} vs. Cu interconnect ρ_{eff} as a function of line-width [5].

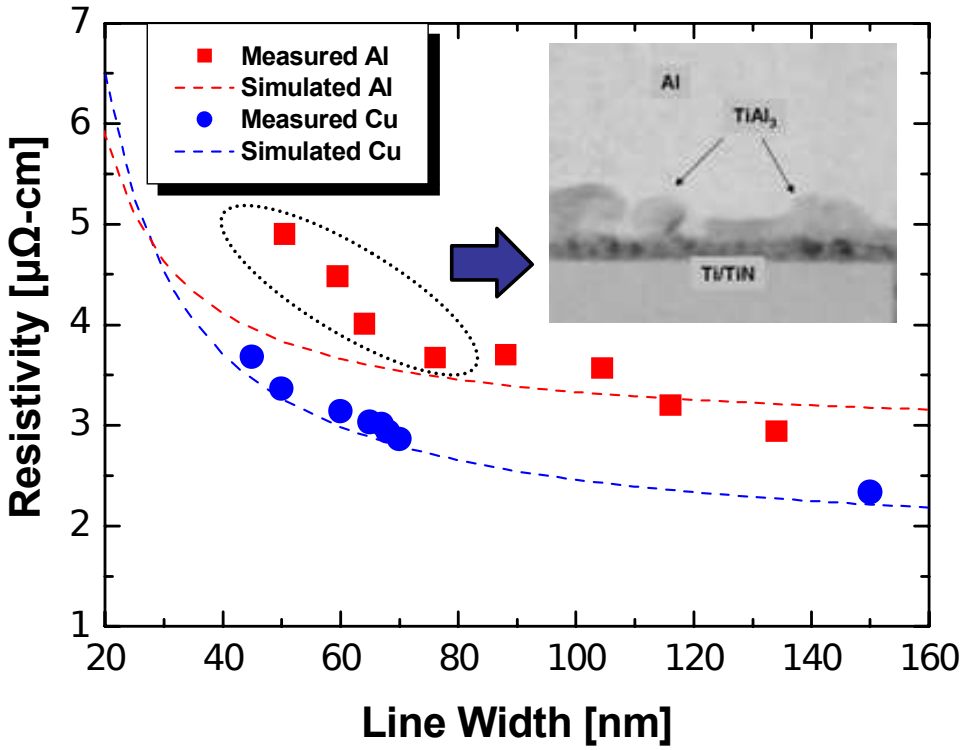

Figure 10: Al interconnect ρ_{eff} vs. Cu interconnect ρ_{eff} as a function of line-width [6].

1.4.4 Semi-Classical Discussion of Electron Scattering

A good illustration of electron scattering considering a long mean free path, λ_{long}, and a short mean free path, λ_{short} can be found in [7] and is presented in Figure 11. Reading each of the illustrations from left to right in Figure 11a, b and c, the first frame represents the length of λ. The second frame is the electron interaction during its course of travel within a metallic grain. The third frame indicates the direction of the electric field **E**.

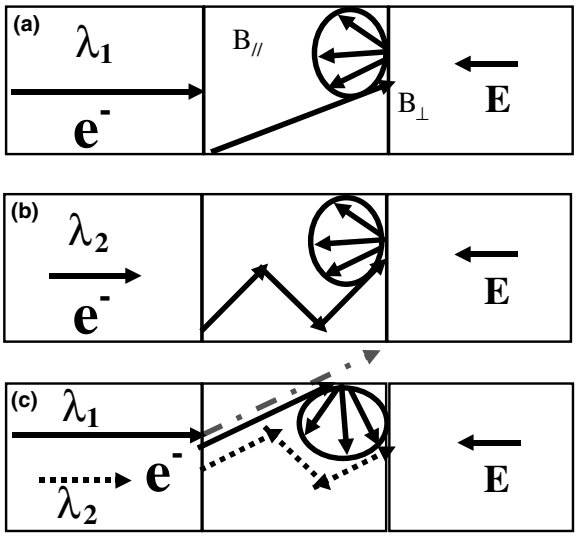

Figure 11: (a) Illustration of scattering for an electron with a λ_{long} within a bulk material. (b) Illustration of scattering for an electron with a λ_{short} within a bulk material experiencing more background scattering (point defect and phonon scattering). (c) Illustrated comparison of scattering for an electron with a λ_{long} (dash-dot line) and an electron with a λ_{short} (dotted line) in a physically limited material. As shown in (c), an electron with a λ_{long} greater than that of a physical dimension will experience more scattering events as the expected distance of travel is interrupted more frequently by scattering sites. Figure from [7].

An electron with a λ_{long} is denoted by a long arrow, whereas an electron with a λ_{short} is denoted by a shorter arrow in the first column. Figure 11c is an illustrated comparison of scattering for an electron with a λ_{long} (dashed-dotted line) and an electron with a λ_{short} (dotted line) in a physically limited material whose dimensions are equal to or less than the length of the longest λ.

The middle frame in each of the illustrations is the electron with some arbitrary trajectory and two boundaries: $B_{\|}$ and $B_{\perp}$. $B_{\|}$ is a boundary parallel to **E**, where $B_{\perp}$ is

a boundary perpendicular to **E**, as described by [105]. The enclosure of these boundaries represents a metallic grain. $B_{\parallel}$ can be either a sidewall or grain boundary, depending on the location of the grain within the interconnect structure. For low resistivity to occur, the electron must reach $B_{\perp}$ without interruption, so it may either diffuse through $B_{\perp}$ to continue conduction or be reflected back into the grain. Increasing the number of scattering events between $B_{\perp}$ (grain boundary) collisions increases resistivity.

In Figure 11a, an electron with a λ_{long} travels a good distance in a large grain before reaching a scattering site, namely, at $B_{\perp}$. At this site, depending on the characteristic of $B_{\perp}$, the electron will diffuse through $B_{\perp}$ or reflect back into the grain itself. In Figure 11b, an electron with a λ_{short} also travels within a large grain while interacting with point defects and phonons before reaching a scattering site, namely, at $B_{\perp}$. It should be noted that the energy loss from electron-phonon interaction has been reported to be on the order of 0.001eV [108], whereas grain boundary diffusion in Cu and Al is 1.2eV and 0.4-0.5eV [109], respectively. In other words, electron-phonon interaction is of little consequence compared to the potential barrier seen at the grain boundary. At this site, depending on the electron interaction with $B_{\perp}$, the electron will diffuse through the boundary or reflect back into the grain itself.

In Figure 11c, the grain size is assumed to be roughly equal to or less than the length of the λ_{long}, and this figure illustrates the impact of the interaction with a parallel boundary $B_{\parallel}$ (e.g. sidewall scattering). In this diagram, the electron with a λ_{long} is represented by dashed-dotted line. For example, the electron could be traveling in copper, where the expected λ_{long}=40 nm. The distance of travel in the physically limiting material is distorted by $B_{\parallel}$, reducing the number of free electrons actually reaching $B_{\perp}$ without interruption, contributing to the increase in resistivity.

Also in Figure 11c, an electron with a λ_{short} is represented by a dotted line. The electron is traveling in a material like Al or AuCu-I, where λ_{Al}=14nm and λ_{CuAu-I}<3nm, respectively. As the electron travels through the grain, it interacts with point defects and phonons, as in Figure 11b. Moreover, unlike an electron in a physically limited material with a λ_{long}, the electron with λ_{short} reaches $B_{\perp}$, increasing the number of free electrons

diffusing through $B_{\perp}$ and reducing the impact of size effects.

Clearly, the λ_{long} could represent an electron in Cu, while the λ_{short} could represent an electron in Al or CuAu-I [110, 111]. Despite background scattering experienced by the electrons and the reduced free electron density, the λ_{short} allows for more electrons to more readily reach $B_{\perp}$ making it less susceptible to size effects as physical dimensions scale below λ_{long}. In summary, for narrow wire widths, the electrons in the λ_{long} materials have a relatively larger increase in the number of scattering events between grain boundary collisions than do λ_{short} materials, which may explain the low values of p found in Table 2. The relative increase means the λ_{long} material's resistivity increases more with narrow wire widths.

1.5 Microprocessor Critical Path Delay

1.5.1 The Critical Path Model

To understand the impact of interconnect process variations, simulations must be performed at the circuit level. Extensive work on determining the maximum critical path delay of a MPU was done by Bowman [8]. A critical path (CP) by definition is the slowest path on a microprocessor and can be modeled as a chain of 2-input NAND gates, with each gate having a fan-out of 3, as seen in Figure 12. A single stage is illustrated in Figure 13.

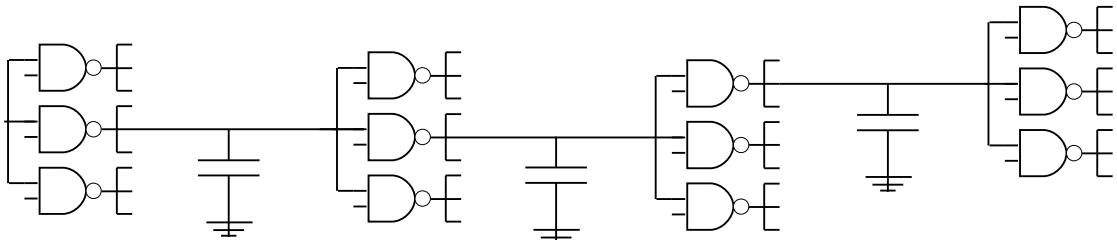

Figure 12: Critical path model from [8], where the interconnect is modeled only as a capacitive parasitic.

The model accounts for only interconnect capacitance within each stage of the CP (Figure 13). It is assumed that a constant number (n_{cp}) of gates exists in the CP and that there are N_{cp} independent CPs per chip. The average wire length (L_{Avg}) that connects the drain of the gate driver to the four gates at the far end is determined using a wire length distribution model [112]. Bowman's work focused only on device D2D and WID variation

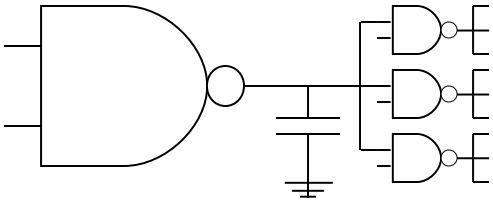

Figure 13: Single-stage of critical path delay model from [8], where the interconnect is modeled only as a capacitive parasitic.

and did not examine the impact of interconnect D2D and WID variation.

1.5.2 Maximum Critical Path Delay

The framework Bowman developed does not account for interconnect RC delay variability arising from interconnect physical variations. Since the transistor and the interconnect delay is expected to change as technology continues to scale [1], it is reasonable to consider a new framework involving interconnect variability. The original framework is illustrated in Figure 14.

Using device models, industry data and other working assumptions, two distributions are created representing the D2D and WID components of variation. In Bowman's case, transistor channel length variation is modeled as normal distributions for the D2D and WID components of variation. Using closed form models, two delay distributions are formed. Since the maximum critical path delay is dictated by the number of independent critical path within a die, the mean delay is typically increased. This increase is also referred to as a mean-shift. This concept will be revisited in Chapter 4. Finally, the D2D and WID distributions are convolved creating a final distribution. As noted in [8], the D2D component largely determines the spread of the final distribution, while the WID component determines the mean of the final distribution.

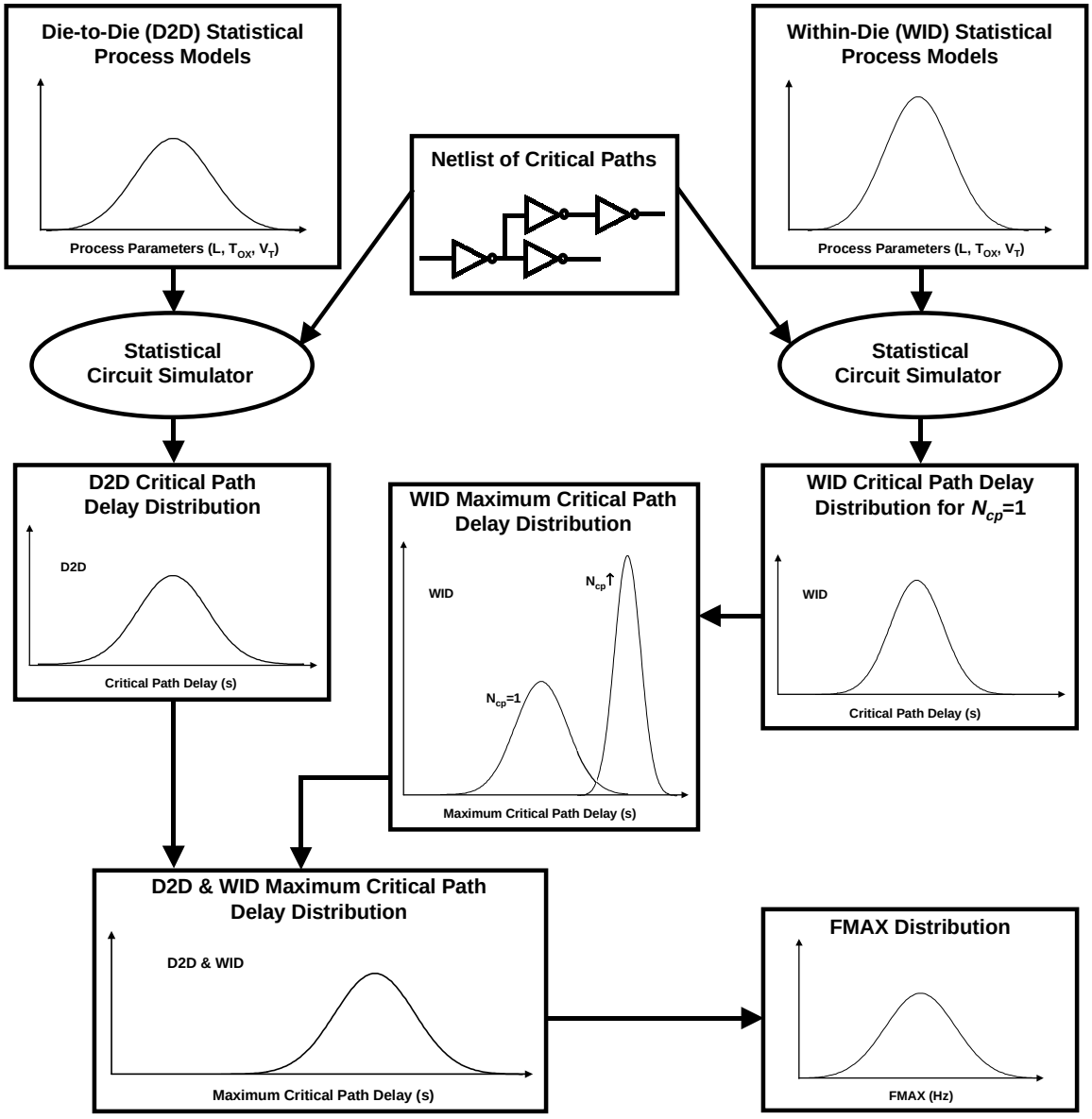

Figure 14: Maximum critical path delay simulation workflow from [8].

1.6 Conclusion

The motivation and background of researching interconnect resistivity is presented in this chapter. The sources of interconnect process variations is reviewed in addition to a semi-classical explanation of a short electron mean free path versus a long electron mean free path. Finally, previous modeling work on interconnect effective resistivity and circuit-level analysis is reviewed to serve a basis on which to improve in this body of work.

CHAPTER II

A NEW PHYSICAL EFFECTIVE RESISTIVITY MODEL

2.1 Introduction

Copper resistivity is expected to increase due to size effects for future technology nodes as line-widths continue below the electron mean free path of copper (λ_{Cu}=40nm) [15]. In this chapter, two original effective resistivity models are presented. The first model was derived by Dr. Reza Sarvari as part of a collaborative effort for this dissertation and was published in [14]. Its contribution is noteworthy as it sets the stage for Task I by offering insight into the derivation of a *new* ρ_{eff} model that includes LER, sidewall specularity and grain boundary reflectivity. In the next two subsections, a model as a function of LER, p and R is derived and verified against simulation data. The new physically-based ρ_{eff} model is then analyzed and used to evaluate ITRS target values for ρ_{eff}, completing Task I.

2.2 Sarvari Model: Line-Edge and Surface Roughness

A closed-form compact ρ_{eff} model in (3), which is derived from [3, 106, 113], was produced as part of a collaborative effort in [14] and is given by

$$\rho_{eff} = \rho_0 \left[\frac{1}{\sqrt{1-(u/w_0)^2}} \left[1 + \frac{\lambda\,(1-p)}{w_0 - (u^2/w_0)} \right] + \frac{1}{\sqrt{1-(v/h_0)^2}} \left[1 + \frac{\lambda\,(1-p)}{w_0 - (v^2/h_0)} \right] - 1 \right] \quad (3)$$

where ρ_0 is the effective bulk conductor resistivity, λ is the electron mean free path, and p is the specularity parameter. The remaining model parameters are defined in Figure 15.

To capture the average behavior of electrons through a conductor, resistivity is derived separately for the horizontal and vertical contributions of surface roughness and surface scattering. The contributions are then combined using Matthiessen's rule. This approach is unlike that in [3], where the numerical analysis included surface roughness and scattering from LER but not CMP dishing. The model is independent of LER period length as it assumes both the vertical and horizontal period lengths are much larger than λ. The

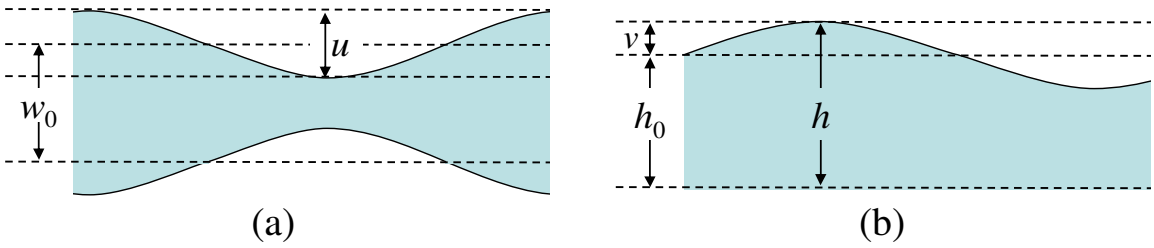

Figure 15: (a) Interconnect LER, where w_0 is the effective line-width and $u/2$ is the amplitude. (b) Interconnect height undulation, where h_0 is the nominal wire height, h is the original height and v is $1/2$ the dishing to occur after CMP.

model in (3), however, does not include grain boundary reflectivity as an additional source of temperature independent scattering. An improved model as a function of LER, sidewall specularity and grain boundary reflectivity is presented in the next section and is the primary contribution of Task I.

2.3 New Physical Model: LER and Size Effects

Although a model for effective resistivity was presented in the previous section, a model as a function of line-edge roughness, surface specularity and grain boundary reflectivity is required to better characterize scattering within a polycrystalline metal interconnect.

2.3.1 Fush-Sondheimer (FS) and Mayadas-Shatzkes (MS) Model

The authors in [2] present an ρ_{eff} model that combines the models for sidewall specularity and grain boundary reflectivity. Individually these models are referred to as the Fuchs-Sondheimer (FS) [106] and the Mayadas-Shatzkes (MS) model [105], respectively. The combined model is known as the FS-MS model. The combination of the two models is possible using Mattheissen's Rule. The FS-MS model is presented in (1) where

$$GB_{scat} = \frac{1}{3}\left[\frac{1}{3} - \frac{\alpha}{2} + \alpha^2 - \alpha^3 \ln\left(1 + \frac{1}{\alpha}\right)\right]^{-1} \tag{4}$$

and

$$SW_{scat} = 0.45\,(1-p)\,\frac{\lambda}{w_0}\left(\frac{1+AR}{AR}\right). \tag{5}$$

In its complete form, the FS-MS model is written as

$$\rho_{eff} = \rho_0\left[\frac{1}{3}\left[\frac{1}{3} - \frac{\alpha}{2} + \alpha^2 - \alpha^3 \ln\left(1 + \frac{1}{\alpha}\right)\right]^{-1} + 0.45\,(1-p)\,\frac{\lambda}{w_0}\left(\frac{1+AR}{AR}\right)\right], \tag{6}$$

where α is given by

$$\alpha = \frac{\lambda}{d}\frac{R}{1-R}; \tag{7}$$

AR (aspect ratio) is given by

$$AR = \frac{h_0}{w_0}; \tag{8}$$

λ is the bulk mean free path of an electron; d is the average separation of the grain boundaries; R is the fraction of electrons scattered by the potential barrier at the grain boundary; p is the fraction of electrons specularly (elastically) scattered at the surface; h_0 is the effective wire thickness; and w_0 is the effective wire width. Even though p and R have physical interpretations, they are very difficult to measure directly. Subsequently, given a physically-based resistivity model, p and R are chosen to provide the best fit to experimental resistivity data. As such, many authors have found different values for p and R for their Cu process (Table 2).

Simulation has already shown that process variations will exacerbate size effects on overall interconnect performance [3, 14, 30]. In [3], the impact of line edge roughness (LER) was numerically modeled. Metrology in [3] revealed that wires with w_0=40nm can have variations as great as 15nm, resulting in widths from 25nm to 55nm along the length of a wire. Henceforth, when referring to LER, 30nm LER (u=30nm) will imply a $\pm$15nm variation along the sidewall of an interconnect; LER and u are used interchangeably. For simplicity, the numerical simulations in [3] assumed that the completely out-of-phase sidewalls exhibited the same undulation amplitude $\frac{u}{2}$ and period a as shown in Figure 16. These assumptions are used to derive the new ρ_{eff} model in the following section. The amount of LER depends on the photolithographic resist technology and CMP process [104] that is used. As a result, LER is assumed to be an inherent and fixed-constant by-product that is superimposed on the metal line-width and independent of the nominal width.

2.3.2 New ρ_{eff} Model Derivation

A model as a function of LER, p and R is required to better characterize scattering within a polycrystalline metal interconnect. Before proceeding to the derivation, let us redefined

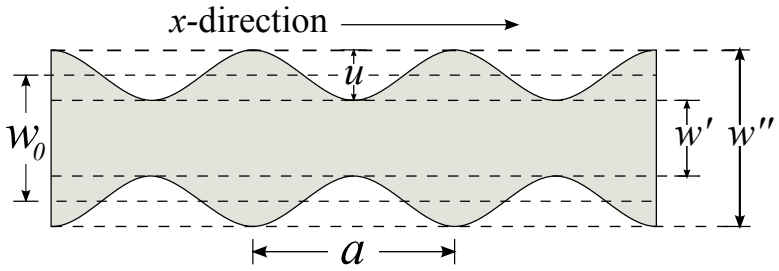

Figure 16: Top view of an interconnect with LER, where w_0 is the effective line-width and $\frac{u}{2}$ is the amplitude. For simplicity, the numerical simulations in [3] assumed that the completely out-of-phase sidewalls exhibited the same undulation amplitude $\frac{u}{2}$ and period a.

(6) in terms of h_0 and w_0 by removing the aspect ratio (AR) dependence. For simplicity, the model in (6) will be written as

$$\rho_{eff} = \rho_0 \left[GB_{scat} + 0.45\,(1-p)\,\frac{\lambda}{w_0}\left(\frac{1+AR}{AR}\right)\right]. \tag{9}$$

First, separate the fractional sum that involves AR as

$$\rho_{eff} = \rho_0 \left[GB_{scat} + 0.45\,(1-p)\,\frac{\lambda}{w_0}\left(\frac{1}{AR}+\frac{AR}{AR}\right)\right]. \tag{10}$$

Second, reduce the term $\frac{AR}{AR}$ to 1.

$$\rho_{eff} = \rho_0 \left[GB_{scat} + 0.45\,(1-p)\,\frac{\lambda}{w_0}\left(\frac{1}{AR}+1\right)\right] \tag{11}$$

Next, given (8), (11) can be re-written as

$$\rho_{eff} = \rho_0 \left[GB_{scat} + 0.45\,(1-p)\,\frac{\lambda}{w_0}\left(\frac{w_0}{h_0}+1\right)\right]. \tag{12}$$

Finally, distribute the term $\frac{1}{w_0}$ into $\left(\frac{w_0}{h_0}+\frac{w_0}{w_0}\right)$, resulting in

$$\rho_{eff} = \rho_0 \left[GB_{scat} + 0.45\lambda\,(1-p)\left(\frac{1}{h_0}+\frac{1}{w_0}\right)\right]. \tag{13}$$

The authors in [3] used numerical approximation to determine the impact of LER. The effect of LER is incorporated by the integration over one LER period as first derived by Namba [113], which is given by

$$\rho_{eff}\,(x) = \frac{1}{a}\int_0^a w_0 \frac{\rho\,(w\,(x)\,,h_0)}{w\,(x)}dx, \tag{14}$$

where ρ is the ρ_{eff} model in (13) from [15] as a function of $w(x)$ and h_0. The function $w(x)$ is the LER and is represented as completely out of phase sidewalls as given by

$$w(x) = w_0 + u \sin\left(\frac{2\pi x}{a}\right), \tag{15}$$

where a is the LER period and $u/2$ is the LER amplitude as illustrated in Figure 16. The model in (14) has also been used in [114] for evaluating transport parameters from the thickness dependence of the conductivity of polycrystalline metal films.

To complete the derivation, the Namba model in (14) must be applied to the resistivity model in (13). By making the assumption that the LER period is much greater than the mean free path of the electron (i.e. $a \gg \lambda$), (14) can be integrated directly. To simply the integration apply a change of variable by letting a=1 and substitute the w_0 term in (13) as $w(x)$ to yield

$$\rho_{eff}(x) = \int_0^1 w_0 \frac{\rho_0 \left[GB_{scat} + 0.45\lambda(1-p)\left(\frac{1}{h_0} + \frac{1}{w(x)}\right)\right]}{w(x)} dx. \tag{16}$$

Before proceeding further, (15) will have w_0 factored out, rewriting (15) as

$$w_0 \times w'(x) = w_0 \left[1 + \frac{u}{w_0} \sin(2\pi x)\right]. \tag{17}$$

Applying (17) to (16), now yields

$$\rho_{eff}(x) = \int_0^1 w_0 \frac{\rho_0 \left[GB_{scat} + 0.45\lambda(1-p)\left(\frac{1}{h_0} + \frac{1}{w_0 \times w'(x)}\right)\right]}{w_0 \times w'(x)} dx. \tag{18}$$

Moving ρ_0 outside the integral and reducing the terms w_0 from the numerator and denominator gives

$$\rho_{eff}(x) = \rho_0 \int_0^1 \frac{\left[GB_{scat} + 0.45\lambda(1-p)\left(\frac{1}{h_0} + \frac{1}{w_0 \times w'(x)}\right)\right]}{w'(x)} dx. \tag{19}$$

Subsequently distributing $\frac{1}{w(x)}$ gives

$$\rho_{eff}(x) = \rho_0 \int_0^1 \left[\frac{GB_{scat}}{w'(x)} + \frac{0.45\lambda(1-p)}{w'(x)}\left(\frac{1}{h_0} + \frac{1}{w_0 \times w'(x)}\right)\right] dx, \tag{20}$$

and again yields

$$\rho_{eff}(x) = \rho_0 \int_0^1 \left[\frac{GB_{scat}}{w'(x)} + 0.45\lambda(1-p)\left(\frac{1}{h_0}\frac{1}{w'(x)} + \frac{1}{w_0 \times w'(x)^2}\right)\right] dx. \tag{21}$$

Separating the integral out now gives

$$\rho_{eff}(x) = \rho_0 \left[GB_{scat} \int_0^1 \frac{dx}{w'(x)} + 0.45\lambda(1-p) \left(\frac{1}{h_0} \int_0^1 \frac{dx}{w'(x)} + \frac{1}{w_0} \int_0^1 \frac{dx}{w'(x)^2} \right) \right]. \quad (22)$$

To complete (22), the integrals $\int_0^1 \frac{dx}{w'(x)}$ and $\int_0^1 \frac{dx}{w'(x)^2}$ must be found. To simplify integration below, let $b = \frac{u}{w_0}$. So for $\int_0^1 \frac{dx}{w'(x)}$

$$\int_0^1 \frac{dx}{w'(x)} = \int_0^1 \frac{dx}{1 + \frac{u}{w_0}\sin(2\pi x)} \Rightarrow \int \frac{dx}{1 + b\sin x} = \frac{2}{\sqrt{1-b^2}} \arctan\left(\frac{\tan\frac{x}{2} + b}{\sqrt{1-b^2}} \right). \quad (23)$$

From the CRC [115],

$$\begin{aligned} \int \frac{dx}{1 + b\sin(2\pi x)} &= \frac{2}{2\pi\sqrt{1-b^2}} \arctan\left(\frac{\tan\frac{2\pi x}{2} + b}{\sqrt{1-b^2}} \right) & (24) \\ &= \frac{1}{\pi\sqrt{1-b^2}} \arctan\left(\frac{\tan\pi x + b}{\sqrt{1-b^2}} \right). & (25) \end{aligned}$$

Evaluating the integral is done by

$$\int_0^1 \frac{dx}{1 + b\sin(2\pi x)} = I_1 + I_2, \quad (26)$$

where

$$I_1 = \frac{1}{\pi\sqrt{1-b^2}} \arctan\left(\frac{\tan\pi x + b}{\sqrt{1-b^2}} \right) \Bigg|_0^{\frac{1}{2}^-} \quad (27)$$

and

$$I_2 = \frac{1}{\pi\sqrt{1-b^2}} \arctan\left(\frac{\tan\pi x + b}{\sqrt{1-b^2}} \right) \Bigg|_{\frac{1}{2}^+}^1. \quad (28)$$

So for I_1

$$\begin{aligned} I_1 &= \frac{1}{\pi\sqrt{1-b^2}} \arctan\left(\frac{\tan\pi x + b}{\sqrt{1-b^2}} \right) \Bigg|_0^{\frac{1}{2}^-} & (29) \\ &= \frac{1}{\pi\sqrt{1-b^2}} \arctan\left(\frac{\tan\frac{\pi}{2}^- + b}{\sqrt{1-b^2}} \right) - \frac{1}{\pi\sqrt{1-b^2}} \arctan\left(\frac{\tan 0 + b}{\sqrt{1-b^2}} \right) & (30) \\ &= \frac{1}{\pi\sqrt{1-b^2}} \arctan\left(\infty^+ \right) - \frac{1}{\pi\sqrt{1-b^2}} \arctan\left(\frac{b}{\sqrt{1-b^2}} \right) & (31) \\ &= \frac{1}{\pi\sqrt{1-b^2}} \left(\frac{\pi}{2} \right) - \frac{1}{\pi\sqrt{1-b^2}} \arctan\left(\frac{b}{\sqrt{1-b^2}} \right). & (32) \end{aligned}$$

So for I_2

$$\begin{aligned} I_2 &= \frac{1}{\pi\sqrt{1-b^2}} \arctan\left(\frac{\tan \pi x + b}{\sqrt{1-b^2}}\right)\Bigg|_{\frac{1}{2}^+}^{1} && (33)\\ &= \frac{1}{\pi\sqrt{1-b^2}} \arctan\left(\frac{\tan \pi + b}{\sqrt{1-b^2}}\right) - \frac{1}{\pi\sqrt{1-b^2}} \arctan\left(\frac{\tan \frac{\pi}{2}^+ + b}{\sqrt{1-b^2}}\right) && (34)\\ &= \frac{1}{\pi\sqrt{1-b^2}} \arctan\left(\frac{b}{\sqrt{1-b^2}}\right) - \frac{1}{\pi\sqrt{1-b^2}} \arctan\left(\infty^-\right) && (35)\\ &= \frac{1}{\pi\sqrt{1-b^2}} \arctan\left(\frac{b}{\sqrt{1-b^2}}\right) - \frac{1}{\pi\sqrt{1-b^2}} \left(-\frac{\pi}{2}\right). && (36) \end{aligned}$$

Combining the terms $I_1 + I_2$ gives

$$\begin{aligned} I_1 + I_2 &= \frac{1}{\pi\sqrt{1-b^2}} \left(\frac{\pi}{2}\right) - \frac{1}{\pi\sqrt{1-b^2}} \arctan\left(\frac{b}{\sqrt{1-b^2}}\right) && (37)\\ &\quad + \frac{1}{\pi\sqrt{1-b^2}} \arctan\left(\frac{b}{\sqrt{1-b^2}}\right) - \frac{1}{\pi\sqrt{1-b^2}} \left(-\frac{\pi}{2}\right) && (38)\\ &= \frac{1}{\pi\sqrt{1-b^2}} \left(\frac{\pi}{2}\right) - \frac{1}{\pi\sqrt{1-b^2}} \left(-\frac{\pi}{2}\right) && (39)\\ &= \pi \frac{1}{\pi\sqrt{1-b^2}} && (40)\\ &= \frac{1}{\sqrt{1-b^2}}. && (41) \end{aligned}$$

Therefore,

$$\int_0^1 \frac{dx}{w'(x)} = \int_0^1 \frac{dx}{1 + \frac{u}{w_0}\sin(2\pi x)} = I_1 + I_2 = \frac{1}{\sqrt{1 - \left(\frac{u}{w_0}\right)^2}}. \tag{42}$$

The following integral in (43) must also be solved.

$$\int_0^1 \frac{dx}{w'(x)^2} = \int_0^1 \frac{dx}{\left[1 + \frac{u}{w_0}\sin(2\pi x)\right]^2} = \int \frac{dx}{(1 + b\sin x)^2} \tag{43}$$

From the CRC [115], it is known that

$$\begin{aligned} \int \frac{dx}{(1 + b\sin x)^2} &= \frac{b\cos x}{(1-b^2)(1 + b\sin x)} + \frac{1}{1-b^2}\int \frac{dx}{1 + b\sin x} && (44)\\ &= \frac{b\cos x}{(1-b^2)(1 + b\sin x)} + \frac{1}{1-b^2}\frac{2}{\sqrt{1-b^2}} \arctan\left(\frac{\tan\frac{x}{2} + b}{\sqrt{1-b^2}}\right). && (45) \end{aligned}$$

Combining $\frac{1}{1-b^2}$ and $\frac{2}{\sqrt{1-b^2}}$ yields

$$\int \frac{dx}{(1 + b\sin x)^2} = \frac{b\cos x}{(1-b^2)(1 + b\sin x)} + \frac{2}{(1-b^2)^{\frac{3}{2}}} \arctan\left(\frac{\tan\frac{x}{2} + b}{\sqrt{1-b^2}}\right) \tag{46}$$

Creating a least common denominator for each addend produces

$$\int \frac{dx}{(1+b\sin x)^2} = \frac{(1-b^2)^{\frac{3}{2}}\, b\cos x}{(1-b^2)^{\frac{3}{2}}\,(1-b^2)\,(1+b\sin x)} \tag{47}$$

$$+\frac{2a\arctan\left(\frac{\tan\frac{x}{2}+b}{\sqrt{1-b^2}}\right)(1-b^2)\,(1+b\sin x)}{(1-b^2)^{\frac{3}{2}}\,(1-b^2)\,(1+b\sin x)}, \tag{48}$$

and combining the sum reduces to

$$\int \frac{dx}{(1+b\sin x)^2} = \frac{(1-b^2)^{\frac{3}{2}}\, b\cos x + 2\arctan\left(\frac{\tan\frac{x}{2}+b}{\sqrt{1-b^2}}\right)(1-b^2)\,(1+b\sin x)}{(1-b^2)^{\frac{3}{2}}\,(1-b^2)\,(1+b\sin x)}. \tag{49}$$

Factoring out (a^2-b^2) and combining the sum reduces to

$$\int \frac{dx}{(1+b\sin x)^2} = \frac{(1-b^2)^{\frac{1}{2}}\, b\cos x + 2\arctan\left(\frac{\tan\frac{x}{2}+b}{\sqrt{1-b^2}}\right)(1+b\sin x)}{(1-b^2)^{\frac{3}{2}}\,(1+b\sin x)}. \tag{50}$$

Correspondingly,

$$\int \frac{dx}{(1+b\sin x)^2} = \int_0^1 \frac{dx}{\left[1+\frac{u}{w_0}\sin(2\pi x)\right]^2} \tag{51}$$

$$= \frac{(1-b^2)^{\frac{1}{2}}\, b\cos 2\pi x + 2\arctan\left(\frac{\tan\pi x+b}{\sqrt{1-b^2}}\right)(1+b\sin 2\pi x)}{2\pi\,(1-b^2)^{\frac{3}{2}}\,(1+b\sin 2\pi x)}. \tag{52}$$

To solve the integral, we must perform the operation

$$\int_0^1 \frac{dx}{\left[1+\frac{u}{w_0}\sin(2\pi x)\right]^2} = I_3 + I_4 \tag{53}$$

where,

$$I_3 = \left.\frac{(1-b^2)^{\frac{1}{2}}\, b\cos 2\pi x + 2\arctan\left(\frac{\tan\pi x+b}{\sqrt{1-b^2}}\right)(1+b\sin 2\pi x)}{2\pi\,(1-b^2)^{\frac{3}{2}}\,(1+b\sin 2\pi x)}\right|_0^{\frac{1}{2}^-} \tag{54}$$

and

$$I_4 = \left.\frac{(1-b^2)^{\frac{1}{2}}\, b\cos 2\pi x + 2\arctan\left(\frac{\tan\pi x+b}{\sqrt{1-b^2}}\right)(1+b\sin 2\pi x)}{2\pi\,(1-b^2)^{\frac{3}{2}}\,(1+b\sin 2\pi x)}\right|_{\frac{1}{2}^+}^1. \tag{55}$$

Solving for I_3 yields

$$I_3 = \frac{(1-b^2)^{\frac{1}{2}}\, b\cos 2\pi\frac{1}{2}^- + 2\arctan\left(\frac{\tan\pi\frac{1}{2}^-+b}{\sqrt{1-b^2}}\right)\left(1+b\sin 2\pi\frac{1}{2}^-\right)}{2\pi\,(1-b^2)^{\frac{3}{2}}\left(1+b\sin 2\pi\frac{1}{2}^-\right)} \tag{56}$$

$$-\frac{(1-b^2)^{\frac{1}{2}}\, b\cos 0 + 2\arctan\left(\frac{\tan 0+b}{\sqrt{1-b^2}}\right)(1+b\sin 0)}{2\pi\,(1-b^2)^{\frac{3}{2}}\,(1+b\sin 0)}. \tag{57}$$

Evaluating terms yields

$$I_3 = \frac{\left(1-b^2\right)^{\frac{1}{2}} b\cos\pi^- + 2\arctan\left(\frac{\tan\frac{\pi}{2}^- + b}{\sqrt{1-b^2}}\right)\left(1+b\sin\pi^-\right)}{2\pi\left(1-b^2\right)^{\frac{3}{2}}\left(1+b\sin\pi^-\right)} \tag{58}$$

$$-\frac{\left(1-b^2\right)^{\frac{1}{2}} b\cos 0 + 2\arctan\left(\frac{\tan 0 + b}{\sqrt{1-b^2}}\right)\left(1+b\sin 0\right)}{2\pi\left(1-b^2\right)^{\frac{3}{2}}\left(1+b\sin 0\right)} \tag{59}$$

$$= \frac{\left(1-b^2\right)^{\frac{1}{2}} b\left(-1\right) + 2\arctan\left(\frac{\infty^+ + b}{\sqrt{1-b^2}}\right)\left(1+0\right)}{2\pi\left(1-b^2\right)^{\frac{3}{2}}\left(1+0\right)} \tag{60}$$

$$-\frac{\left(1-b^2\right)^{\frac{1}{2}} b\left(1\right) + 2\arctan\left(\frac{0 + b}{\sqrt{1-b^2}}\right)\left(1+0\right)}{2\pi\left(1-b^2\right)^{\frac{3}{2}}\left(1+b\sin 0\right)} \tag{61}$$

$$= \frac{\left(-b\right)\left(1-b^2\right)^{\frac{1}{2}} + 2\left(\frac{\pi}{2}\right)}{2\pi\left(1-b^2\right)^{\frac{3}{2}}} - \frac{b\left(1-b^2\right)^{\frac{1}{2}} + 2\arctan\left(\frac{b}{\sqrt{1-b^2}}\right)}{2\pi\left(1-b^2\right)^{\frac{3}{2}}} \tag{62}$$

$$= \frac{-b\left(1-b^2\right)^{\frac{1}{2}} + \pi}{2\pi\left(1-b^2\right)^{\frac{3}{2}}} - \frac{b\left(1-b^2\right)^{\frac{1}{2}} + 2\arctan\left(\frac{b}{\sqrt{1-b^2}}\right)}{2\pi\left(1-b^2\right)^{\frac{3}{2}}}. \tag{63}$$

Solving for I_4 yields

$$I_4 = \frac{b\left(1-b^2\right)^{\frac{1}{2}}\cos 2\pi + 2\arctan\left(\frac{\tan\pi + b}{\sqrt{1-b^2}}\right)\left(1+b\sin 2\pi\right)}{2\pi\left(1-b^2\right)^{\frac{3}{2}}\left(1+b\sin 2\pi\right)} \tag{64}$$

$$-\frac{b\left(1-b^2\right)^{\frac{1}{2}}\cos 2\pi\tfrac{1}{2}^+ + 2\arctan\left(\frac{\tan\pi\frac{1}{2}^+ + b}{\sqrt{1-b^2}}\right)\left(1+b\sin 2\pi\frac{1}{2}^+\right)}{2\pi\left(1-b^2\right)^{\frac{3}{2}}\left(1+b\sin 2\pi\frac{1}{2}^+\right)}. \tag{65}$$

Evaluating terms yields

$$I_4 = \frac{b\left(1-b^2\right)^{\frac{1}{2}}\left(1\right) + 2\arctan\left(\frac{0 + b}{\sqrt{1-b^2}}\right)\left(1+0\right)}{2\pi\left(1-b^2\right)^{\frac{3}{2}}\left(1+0\right)} \tag{66}$$

$$-\frac{b\left(1-b^2\right)^{\frac{1}{2}}\cos\pi^+ + 2\arctan\left(\frac{\tan\frac{\pi}{2}^+ + b}{\sqrt{1-b^2}}\right)\left(1+b\sin\pi^+\right)}{2\pi\left(1-b^2\right)^{\frac{3}{2}}\left(1+b\sin\pi^+\right)} \tag{67}$$

$$= \frac{b\left(1-b^2\right)^{\frac{1}{2}} + 2\arctan\left(\frac{b}{\sqrt{1-b^2}}\right)}{2\pi\left(1-b^2\right)^{\frac{3}{2}}} - \frac{b\left(1-b^2\right)^{\frac{1}{2}}\left(-1\right) + 2\arctan\left(\frac{\infty^- + b}{\sqrt{1-b^2}}\right)\left(1+0\right)}{2\pi\left(1-b^2\right)^{\frac{3}{2}}\left(1+0\right)} \tag{68}$$

$$= \frac{b\left(1-b^2\right)^{\frac{1}{2}} + 2\arctan\left(\frac{b}{\sqrt{1-b^2}}\right)}{2\pi\left(1-b^2\right)^{\frac{3}{2}}} - \frac{-b\left(1-b^2\right)^{\frac{1}{2}} + 2\left(-\frac{\pi}{2}\right)}{2\pi\left(1-b^2\right)^{\frac{3}{2}}} \tag{69}$$

$$= \frac{b\left(1-b^2\right)^{\frac{1}{2}} + 2\arctan\left(\frac{b}{\sqrt{1-b^2}}\right)}{2\pi\left(1-b^2\right)^{\frac{3}{2}}} - \frac{-b\left(1-b^2\right)^{\frac{1}{2}} - \pi}{2\pi\left(1-b^2\right)^{\frac{3}{2}}}. \tag{70}$$

Combining $I_3 + I_4$ reduces to

$$
\begin{aligned}
I_3 + I_4 &= \frac{-b\left(1-b^2\right)^{\frac{1}{2}} + \pi}{2\pi\left(1-b^2\right)^{\frac{3}{2}}} - \frac{b\left(1-b^2\right)^{\frac{1}{2}} + 2\arctan\left(\frac{b}{\sqrt{1-b^2}}\right)}{2\pi\left(1-b^2\right)^{\frac{3}{2}}} && (71)\\
&\quad + \frac{b\left(1-b^2\right)^{\frac{1}{2}} + 2\arctan\left(\frac{b}{\sqrt{1-b^2}}\right)}{2\pi\left(1-b^2\right)^{\frac{3}{2}}} - \frac{-b\left(1-b^2\right)^{\frac{1}{2}} - \pi}{2\pi\left(1-b^2\right)^{\frac{3}{2}}} && (72)\\
&= \frac{-b\left(1-b^2\right)^{\frac{1}{2}} + \pi}{2\pi\left(1-b^2\right)^{\frac{3}{2}}} - \frac{-b\left(1-b^2\right)^{\frac{1}{2}} - \pi}{2\pi\left(1-b^2\right)^{\frac{3}{2}}} && (73)\\
&= \frac{-b\left(1-b^2\right)^{\frac{1}{2}} + \pi}{2\pi\left(1-b^2\right)^{\frac{3}{2}}} + \frac{b\left(1-b^2\right)^{\frac{1}{2}} + \pi}{2\pi\left(1-b^2\right)^{\frac{3}{2}}} && (74)\\
&= \frac{-b\left(1-b^2\right)^{\frac{1}{2}} + \pi + b\left(1-b^2\right)^{\frac{1}{2}} + \pi}{2\pi\left(1-b^2\right)^{\frac{3}{2}}} && (75)\\
&= \frac{2\pi}{2\pi\left(1-b^2\right)^{\frac{3}{2}}} && (76)\\
&= \frac{1}{\left(1-b^2\right)^{\frac{3}{2}}}. && (77)
\end{aligned}
$$

Therefore,

$$
\int_0^1 \frac{dx}{w\left(x\right)^2} = \int_0^1 \frac{dx}{\left[1 + \frac{u}{w_0}\sin\left(2\pi x\right)\right]^2} = I_3 + I_4 = \frac{1}{\left[1 - \left(\frac{u}{w_0}\right)^2\right]^{\frac{3}{2}}}. \tag{78}
$$

Finally, substituting (42) and (78) into (22), yields

$$
\begin{aligned}
\rho_{eff} &= \rho_0\left[\frac{GB_{scat}}{\sqrt{1-\left(\frac{u}{w_0}\right)^2}} + 0.45\lambda\left(1-p\right)\left(\frac{1}{h_0}\frac{1}{\sqrt{1-\left(\frac{u}{w_0}\right)^2}} + \frac{1}{w_0}\frac{1}{\left[1-\left(\frac{u}{w_0}\right)^2\right]^{\frac{3}{2}}}\right)\right] && (79)\\
&= \rho_0\left[\frac{GB_{scat}}{\sqrt{1-\left(\frac{u}{w_0}\right)^2}} + 0.45\lambda\left(1-p\right)\left(\frac{1}{\sqrt{1-\left(\frac{u}{w_0}\right)^2}}\right)\left(\frac{1}{h_0} + \frac{1}{w_0}\frac{1}{1-\left(\frac{u}{w_0}\right)^2}\right)\right] && (80)\\
&= \frac{\rho_0}{\sqrt{1-\left(\frac{u}{w_0}\right)^2}}\left[GB_{scat} + 0.45\lambda\left(1-p\right)\left(\frac{1}{h_0} + \frac{1}{w_0}\frac{1}{1-\left(\frac{u}{w_0}\right)^2}\right)\right] && (81)\\
&= \frac{\rho_0}{\sqrt{1-\left(\frac{u}{w_0}\right)^2}}\left[GB_{scat} + 0.45\lambda\left(1-p\right)\left(\frac{1}{h_0} + \frac{1}{w_0\left[1-\left(\frac{u}{w_0}\right)^2\right]}\right)\right]. && (82)
\end{aligned}
$$

A closed-form of (82) in terms of aspect ratio (AR) can be written as

$$
\rho_{eff} = \frac{\rho_0}{\sqrt{1-\left(\frac{u}{w_0}\right)^2}}\left[GB_{scat} + 0.45\left(1-p\right)\frac{\lambda}{w_0}\left(\frac{1}{AR} + \frac{1}{1-\left(\frac{u}{w_0}\right)^2}\right)\right] \tag{83}
$$

Table 3: New ρ_{eff} Model Parameter Definitions

Parameter	Definition
ρ_0	Effective bulk resistivity
u	Line-edge roughness (LER)
w_0	Interconnect width
h_0	Interconnect height
AR	Aspect ratio defined as $\frac{h_0}{w_0}$
λ	Electron mean free path
p	Sidewall specularity
GB_{scat}	Grain boundary scattering model: $G(\alpha) = \frac{1}{3}\left[\frac{1}{3} - \frac{\alpha}{2} + \alpha^2 - \alpha^3 \ln\left(1 + \frac{1}{\alpha}\right)\right]^{-1}$
α	$\frac{\lambda}{d}\frac{R}{1-R}$
d	Average distance between grain boundaries (assumed to be independent of w_0)
R	Grain boundary reflectivity

with its model parameters are defined in Table 3.

The derivation is complete by having applied the Namba model in (14) to the ρ_{eff} model in (6). This results in a new closed-form expression for the effective resistivity and is given in (82) or (83). All simulation results presented in Task III characterize electron scattering using (82). In the next section the model will be verified against numerical simulation data from [3].

2.3.3 Model Verification to Numerical Simulation

In Figure 17, the new physically-based ρ_{eff} model in equation (82) is compared to numerical simulations from [3] and agrees well for a range of w_0 and LER. Notice as w_0 approaches u along the x-axis, the effective resistivity begins to increase exponentially. This increase is due to the LER becoming a large percentage of the w_0, especially as the w_0 scales down, while the LER remains fixed.

While agreement to numerical simulation data confirms validation of the new ρ_{eff} model, empirical measurements of fabricated sub-100nm copper and aluminum interconnects will be used to calibrate the new model in Task V. Measurements will include average LER seen across the chip for varying effective line-widths. By pre-determining the average LER using top-down SEM measurements, R and p will be determined for best fit.

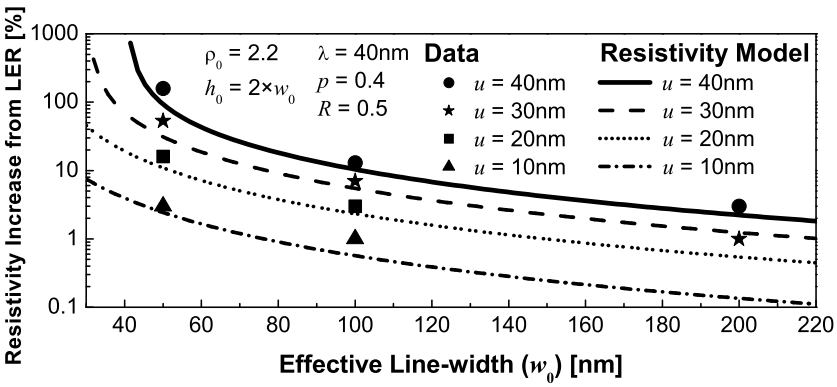

Figure 17: Comparison of new resistivity model projections in equation (82) with numerical simulations from [3] for a range of w_0 and LER, where $u/2$ is the amplitude. The model in (82) is a function of LER, sidewall specularity and grain boundary scattering. Average grain size is considered to be equal to the effective line-width w_0 [9, 10].

2.4 Model Analysis

To further appreciate the new model derived in this dissertation, an analysis of its limits and its impact on ITRS projections are discussed in this section. The limits on w_0 have clear physical interpretations. The physical interpretation of the new ρ_{eff} model greatly impacts the projections made in the ITRS. With LER, ρ_{eff} has a pronounced sensitivity to the $p$and R values that are chosen.

2.4.1 Physical Interpretation of the Limits on w_0

As we would expect physically, the new model predicts that as the LER, which is represented by the variable u, approaches the w_0, $\rho_{eff} \rightarrow \infty$. As depicted in Figure 18, in the limit as $u \rightarrow w_0$, pinching in the wire occurs resulting in an open circuit.

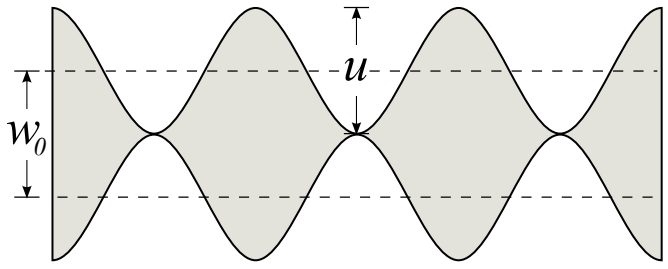

Figure 18: An interconnect with the LER (u) equal to the effective line-width w_0.

At the other extreme, when the LER variable is set to zero, the new model in equation

(82) appropriately collapses to the original FS-MS model in (6). For this case, the interconnect is ideal with straight edges running in parallel as shown in Figure 19. This is the same configuration that is assumed when using the FS-MS model for estimating projections in the ITRS.

Figure 19: An ideal interconnect with no LER.

Examining the model further, equation (83) can be rewritten as

$$\rho_{eff} = \rho_0 \, LER_{\rho_0} \left[GB_{scat} + 0.45\,(1-p)\,\frac{\lambda}{w_0}\left(\frac{1}{AR} + LER_{SW}\right)\right], \tag{84}$$

where

$$LER_{\rho_0} = \frac{1}{\sqrt{1-\left(\frac{u}{w_0}\right)^2}} \tag{85}$$

and

$$LER_{SW} = \frac{1}{1-\left(\frac{u}{w_0}\right)^2}. \tag{86}$$

Using these definitions clearly show that integrating the FS-MS model over one LER period results in a simple modification to the original model in (11).

The first additional term, LER_{ρ_0}, increases the overall ρ_{eff} due to LER. Assuming size effects are negligible in (84) with R=0 and p=1, the new model indicates that LER would still increase ρ_{eff}, especially if the LER is a significant value to that of the w_0. A plot of the percent increase of LER_{po} can be found in Figure 20 as the dashed black curve, where LER_{po} increases the overall ρ_{eff} due to LER. The magnitude is bounded between 0 and 1 or from 0nm LER to where LER = w_0. When the LER accounts for 70.7% of the w_0, the ρ_{eff} can be expected to double (or increase by 100%) as indicated in Figure 20, assuming no size effects.

The second change to the model in (11) is seen in the sidewall scattering component of (84). The original model in (11) indicated that as $AR \rightarrow \infty$ (i.e., $\frac{h_0}{w_0} \rightarrow \infty$), the

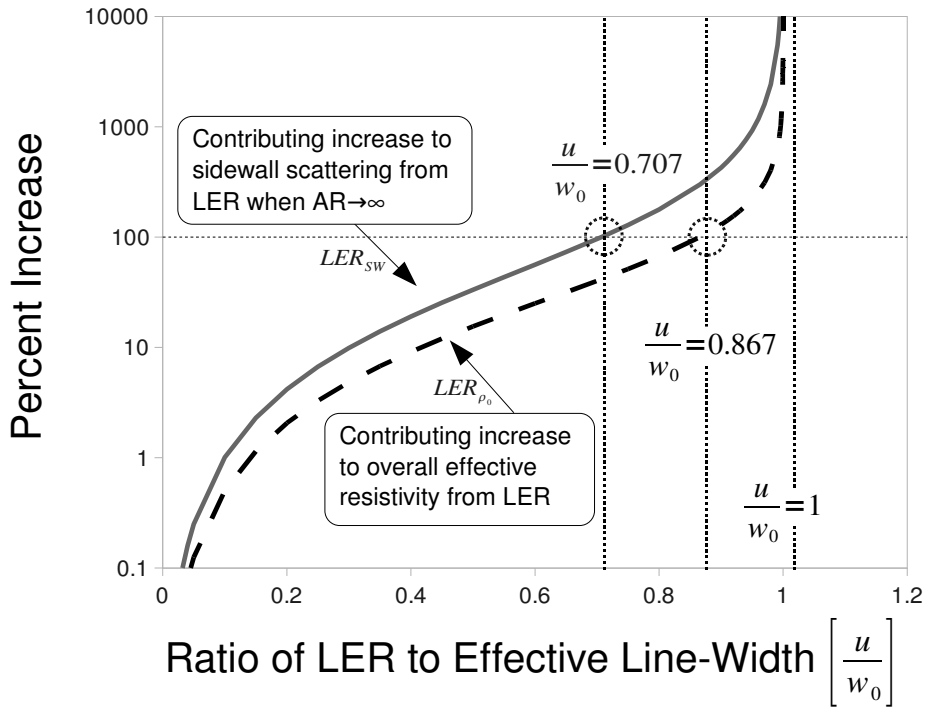

Figure 20: Mapping of $\frac{u}{w_0}$ to percent increase to ρ_0 and SW_{scat}. The magnitudes of increase is bounded between 0 and 1 or from 0nm LER to where LER = w_0.

impact of the aspect ratio can be considered negligible to increasing the contribution of specular scattering. However, the addition of LER_{SW} in equation (84) implies that while $AR \to \infty$, the LER increases the contribution of sidewall scattering especially as $u \to w_0$. Assuming $AR = \infty$, the increase to the contribution of sidewall scattering can double when $u/w_0 \approx 86.7\%$ as shown in Figure 20 as the solid grey curve, where the increase is a function of u/w_0. The magnitude of increase is bounded between 0 and 1 or from 0nm LER to where LER = w_0. To mitigate the impact and overall contribution of sidewall scattering with LER, any opportunity to increase the number of elastic collisions along the sidewall (where $p \to 1$) should be exploited. Since ideal cases have been used to appreciate the physical impact of LER using (84) on ρ_{eff}, the next section will demonstrate the impact of LER on ρ_{eff} assuming different scattering values for p and R for the ITRS 2007 projections.

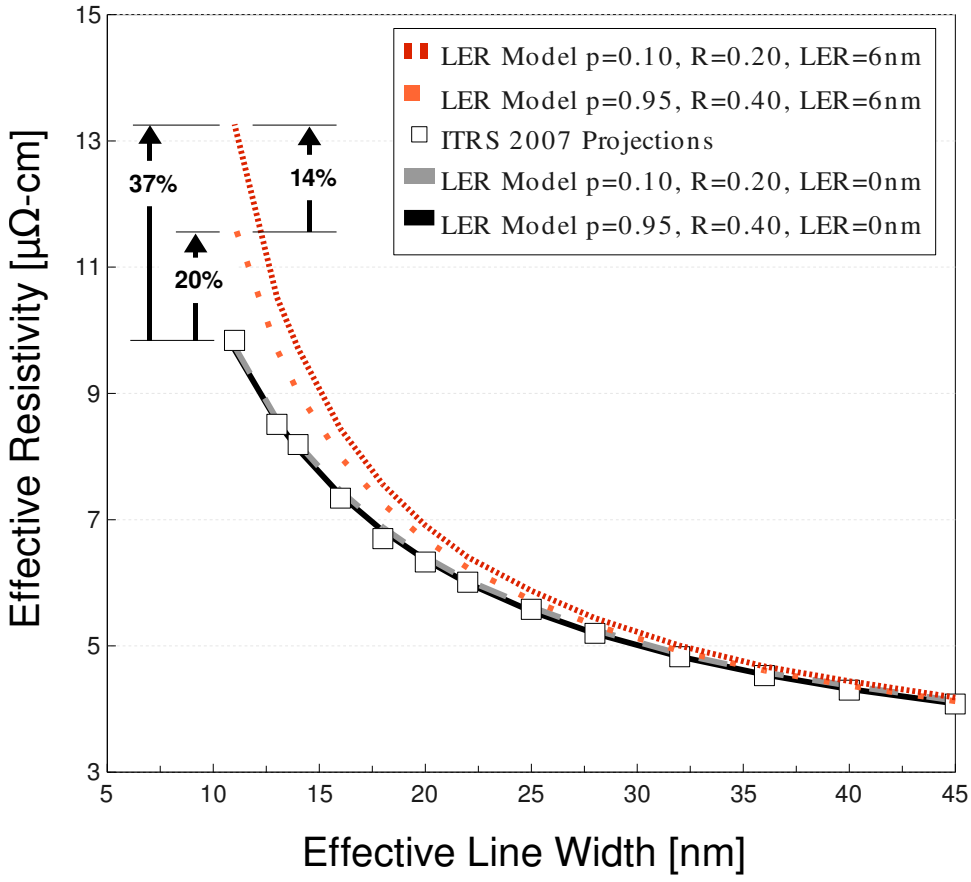

Figure 21: Comparing the impact of different scattering parameter pair values with fixed LER for 2007 ITRS projections.

2.4.2 Impact of LER and Size Effects on ITRS 2007 Targets

This section will demonstrate the impact of different p and R value pairs for ITRS ρ_{eff} targets. The ITRS 2007 ρ_{eff} target values are plotted in Figure 21. Two different pairs of p and R values are used to best fit the values with no LER as plotted in the solid black line (p=0.95, R=0.40) and the dashed grey line (p=0.10, R=0.20). The algorithm used to determine these scattering parameters is described in greater detail in Chapter 4.

When the LER is increased from 0nm to 6nm, there is a noticeable impact of LER at the 11nm node (2022); however the magnitudes of the impact are different. Not surprisingly, there is the smallest impact (20% increase from ITRS ρ_{eff} values) from LER when p=0.95, whose p-value is closest to 1, as seen in the dotted orange line. In this case, size effects results largely from grain boundary scattering. However, when p is closer to 0, where p=0.10

and R=0.20, there is a greater impact from LER as shown in the tightly-dotted red line. This increase in ρ_{eff} maps to a 37% increase from ITRS ρ_{eff} values at the 11nm node or a 14% increase from the dotted orange line, where p=0.95 and R=0.40. To conclude, a low p value causes greater impact from LER. Finally, as this exercise demonstrates, scattering values must be carefully chosen since the impact of LER on ρ_{eff} is sensitive to the p and R values chosen.

2.5 Conclusion

Collaborative efforts in [14] have been extended into a new resistivity model as a function of LER, sidewall specularity and grain boundary reflectivity. The new model in (82) is a closed-form expression derived by integrating over a single LER period. The new model will be especially useful for the fast interconnect statistical simulator to be described in Task III. The new ρ_{eff} model agrees well to numerical simulation data and offers clear physical insight to the impact of LER on ρ_{eff}. Caution should be taken when selecting the scattering parameter values to best fit data ρ_{eff} projections as the response to LER can vary dramatically. In Chapter 6, the new ρ_{eff} model will be calibrated to real ρ_{eff} values.

CHAPTER III

NEW CRITICAL PATH MODEL INCLUDING SIZE EFFECTS AND LINE-EDGE ROUGHNESS

3.1 Introduction

In chapter 2, Task I of this work was fulfilled by the derivation and analysis of the new physical ρ_{eff} model. In this chapter, Task II is accomplished through the enhancement of the former critical path (CP) delay model presented by Bowman in [8]. The enhancement is necessary since the Bowman model only accounts for interconnect parasitic capacitance; however, interconnect ρ_{eff} is increasing due to size effects as interconnect dimensions scale well beyond the mean free path of electrons in copper, λ_{Cu}. The establishment of a new CP model is critical to Task III, which is to develop a statistical simulation framework and is presented in chapter 4. In the follow sections, the new single stage CP (SSCP) model, average wire-length projections, transistor resistance estimation and interconnect resistance with size effects are discussed.

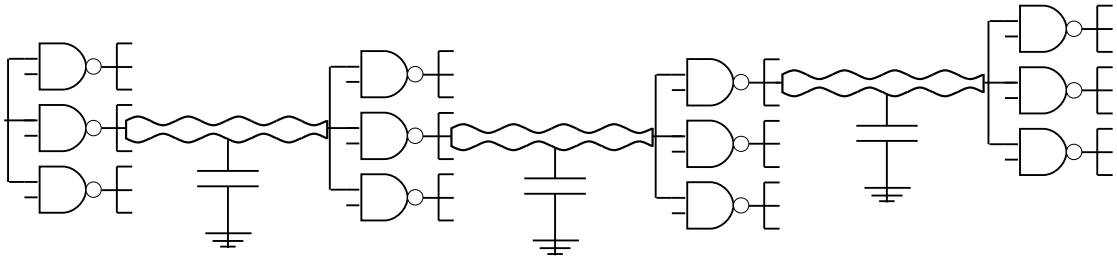

Figure 22: Enhanced critical path model with interconnect RC parasitics.

3.2 The New Single Stage Critical Path (CP) Model

By definition, a CP is the slowest path in a microprocessor. A new CP model is constructed from a chain of 2-input NAND gates with each driving gate having a fan-out of 3 as seen in Figure 22. A single stage is illustrated in Figure 23. The new CP delay model distinguishes

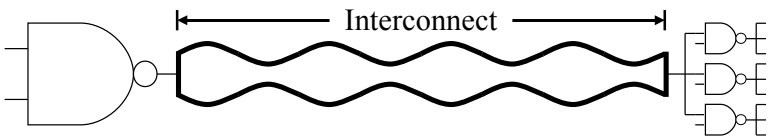

Figure 23: Enhanced single-stage of critical path delay model with interconnect resistance (using LER and size effects) and capacitance.

itself from its Bowman counterpart (illustrated in Figure 12) by accounting for interconnect resistance (R_{int}) and capacitance (C_{int}) within each stage of the CP. R_{int} is calculated in (87), where ρ_{eff} is the new model in (82); l_{int} is the interconnect length; and h_0 is the nominal line height. C_{int} is calculated using capacitance models presented in [11, 12] and its final form is shown in (88), where ϵ_{ox} is the dielectric constant of the insulator calculated in (89); ϵ_r is the relative dielectric constant obtained from [1]; ϵ_o is the permittivity of free space ($8.854E$-14 F/cm); t_{ox} is the oxide thickness; and s is the spacing between interconnects. In this work, it is assumed that s=w_0 and t_{ox}=h_0. In [12], Sakurai presents a 50% delay ($t_{0.5}$) model in (90) that will be used in this work to calculate the RC delay of a single stage of a CP, where R_T and C_T are defined in (91) and (92), respectively.

$$R_{int} = \frac{\rho_{\mathit{eff}} l_{int}}{w_0 h_0} \tag{87}$$

$$C_{int} = \epsilon_{ox} l_{int} \left[2.8 \left(\frac{h_0}{t_{ox}} \right)^{0.222} + 1.15 \frac{w_0}{t_{ox}} + 2 \left(0.83 \frac{h_0}{t_{ox}} - 0.07 \left(\frac{h_0}{t_{ox}} \right)^{0.222} + 0.03 \frac{w_0}{t_{ox}} \right) \left(\frac{s}{t_{ox}} \right)^{-1.34} \right] \tag{88}$$

$$\epsilon_{ox} = \epsilon_r \epsilon_o \tag{89}$$

$$t_{0.5} = R_{int} C_{int} \left[0.377 + 0.693 \left(R_T C_T + R_T + C_T \right) \right] \tag{90}$$

$$R_T = \frac{R_t}{R_{int}} \tag{91}$$

$$C_T = \frac{C_t}{C_{int}} \tag{92}$$

Figure 24 illustrates the mapping of each of the components needed to calculate the single-stage RC delay. Transistor parasitics R_t (transistor resistance) and C_t (transistor capacitance) will be determined using ITRS 2007 Process Integration, Devices and Structures projected values of saturation current ($I_{d,sat}$), power supply (V_{dd}) and gate capacitance per unit width ($C_{g,total}$). C_t will be calculated as

$$C_t = FO_n \left[(C_{g,total}) (W_n) + (C_{g,total}) (W_p) \right], \tag{93}$$

where FO_n is the fanout seen by the driving gate in a single stage of a CP; W_n is the width of the nFET transistor at the end of the stage; and W_p is the width of the pFET transistor at the end of the stage. For gate sizing, a PN ratio of 2 is assumed with the W/L ratio of 20, which is considered a typical value [83]. For completeness, the values for $I_{d,sat}$, V_{dd} and $C_{g,total}$ from [1] are presented in Table 4. Since the the IV characteristic of a transistor is non-linear, a survey of foundry data will be used to determine the best approach for estimating R_t.

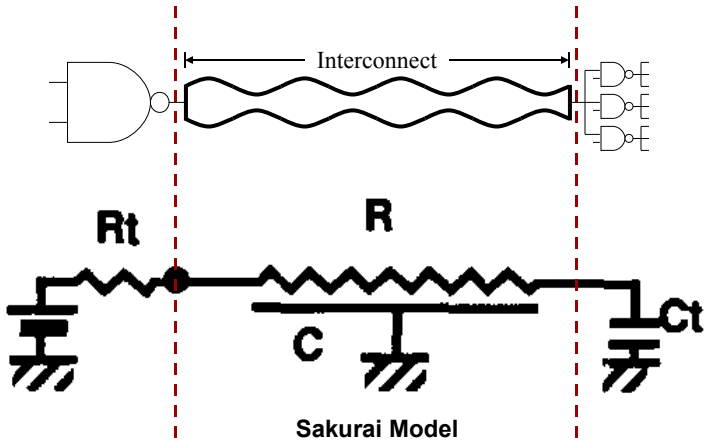

Figure 24: Circuit-level estimation of a single-stage critical path delay with interconnect resistance using Sakurai's model [11, 12].

The number stages in a CP (n_{cp}) will be used to distinguish between a single core (sCore) and multi-core (mCore) MPU. According to [83], sCore architectures can assume n_{cp}=8 and a relaxed value of n_{cp}=16 for multi-core (mCore) systems. In order to meet throughput requirements, an sCore CP must be shorter (smaller n_{cp}), where mCore designs can meet the same throughput at a slower speed (larger n_{cp}). The number of cores in an

Table 4: ITRS 2007 Values for Transistor and Interconnect Parasitic Estimation

Year	w_0	ϵ_r	V_{dd}[V]	$I_{d,sat}\left[\frac{\mu A}{\mu m}\right]$	$C_{g,total}\left[\frac{C}{\mu m}\right]$	# Tx $\left[\frac{millions}{mm^2}\right]$	Chipsize [mm^2]
2007	68	3.3	1.1	1211	7.10E-16	154	280
2010	45	2.9	1.0	1807	8.40E-16	309	280
2013	32	2.8	0.90	2109	6.58E-16	617	280
2016	22	2.5	0.80	2627	5.07E-16	1235	280
2019	16	2.3	0.70	2768	4.10E-16	2469	280
2022	11	2.0	0.65	2786	3.42E-16	4938	280

mCore system is determined by starting with 4 cores in 2007 and increasing this value 1.4X per technology node [1] and are assumed to operate at the same frequency. The number of cores will be used in determining the average wire-length in the next section.

3.3 Single Stage Average Wire-Length Projections

To model interconnect RC parasitics, the length of wire needed to connect the driver to the 3 gates at the end of the wire must be calculated. For this work, the average wire-length (L_{Avg}) is used and calculated using the wire-length distribution model in [112], the ITRS high-volume MPU parameters [1] and a Rent's parameter of 0.7. The selection of the Rent's parameter value of 0.7 is based on the extensive body of work done on Rent's Rule [112, 116–121], whose published empirical values are <1.0 and typically within a range of 0.5-0.8. Some of the latest and in-depth published work on Rent's Rule is presented by Lanzerotti et al. [117–119] on the random logic macros of the dual-core POWER4 microprocessor with values ranging from 0.31-0.69. The larger the value of the Rent's exponent, the more complex the circuit. Considering the increasing complexity of design as the number of transistors on a die increases per generation, 0.7 was chosen to sufficiently describe the complexity of future systems. The full equation for L_{Avg} is given below as

$$L_{Avg} = \left(N^{(p_{Rent}-0.5)}\right)\left[\frac{p_{Rent}+1-4^{(p_{Rent}-0.5)}}{2\left(p_{Rent}-0.5\right)\left(p_{Rent}+0.5\right)\left(p_{Rent}\right)}\right], \tag{94}$$

where N is the number of blocks in a core and p_{Rent} is the Rent's exponent. L_{Avg} per core is calculated in gate pitches, where a gate pitch is the average center-to-center spacing

between two gates. Absolute wire length is calculated by obtaining the gate pitch, which is the square root of the gate area, given by $A \times F^2$, where A is the cell area factor and F is the ITRS MPU half-pitch per year [1]. The calculated L_{Avg} values are plotted in Figure 25 using chip size and transistor count information from Table 4. As expected, mCore designs enable shorter average wire lengths as compared to sCore designs, since each core has a smaller footprint that its sCore counterpart. In the next section, a survey of device resistance estimation is discussed.

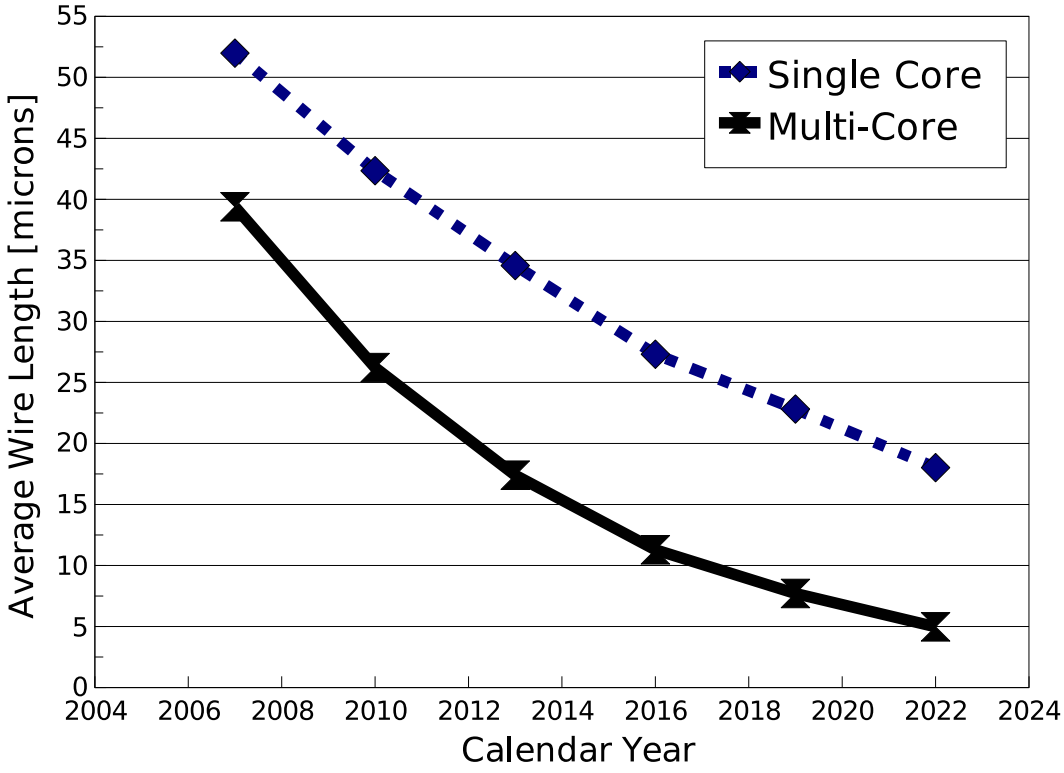

Figure 25: The graph above plots the average wire length (L_{Avg}) for single and multi-core chips versus calendar year. A constant number (n_{cp}) of gates in the CP with n_{cp}=8 for single core (sCore) systems and a relaxed value of n_{cp}=16 for multi-core (mCore) systems is assumed. The number of cores in an mCore system is determined by starting with 4 cores in 2007 and increasing this value 1.4X per technology node [1].

3.4 Device Resistance Verification

A circuit-level approach in estimating transistor operating resistance using foundry data from MOSIS [122] is provided. Without such an approach, computationally heavier simulations, such as Monte Carlo simulations in HSPICE using BSIM3 models [123, 124], would require exhaustively more time to obtain results. Moreover, while BSIM3 models have been used in predictive device modeling [125], timing analysis [126], yield estimation [127], statistical circuit simulation [36] and overall circuit optimization [128, 129], the focus of this work is strictly on interconnect process variations, leaving extensive transistor analysis beyond the scope of this research. In evaluating the approximate operating resistance of a transistor, the method of linearly approximating the device IV behavior is applied. This method finds the inverse slope between two points on an IV curve, thus approximating the device resistance using the schematic shown in Figure 26.

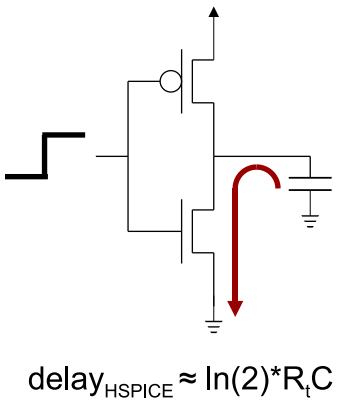

Figure 26: HSPICE 50% delay estimation using a 2pF capacitive load.

The two points of interest are the origin and the current at 75% of V_{dd} in Figure 27, where the approximate nominal device resistance (R_t) is given by

$$R_t = \frac{0.75V_{dd}}{I_{d,sat}}. \tag{95}$$

The current at 75% of V_{dd} was chosen arbitrarily. The approximate nominal device resistance in (95) can be used to estimate the 50% delay ($\tau_{50\%}$) of an NFET charging a capacitive load, which is given by

$$\tau_{50\%} = \ln(2)R_tC_{load} \approx \frac{1}{2}\frac{C_{load}V_{dd}}{I_{d,sat}}, \tag{96}$$

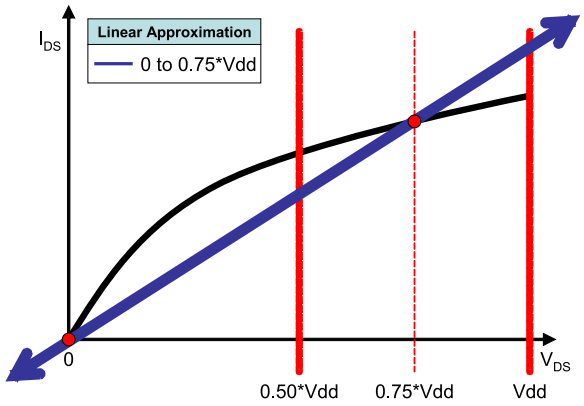

Figure 27: HSPICE device resistance estimation using 75% V_{dd}.

where C_{load} is the capacitive load seen by the device; V_{dd} is the supply voltage; and $I_{d,sat}$is the saturation current. This model is verified using 237 process decks from MOSIS IBM and MOSIS TSMC runs across different technology generations. It is shown that close approximation between the 50% delay of an NFET and an equivalent 50% RC delay model in (96) with an ideal input voltage source is obtainable. Device width is assumed to be 20 times that of the drawn gate length (ITRS half-pitch), while the PFET to NFET ratio is assumed to be 2. In total, 131 IBM and 106 TSMC technology decks were analyzed. For the IBM 500nm, 350nm, 250nm, 180nm, and 130nm technologies, 18, 9, 13, 71, and 20 models were evaluated respectively in the stated manner driving a 2pF capacitive load. The 2pF capacitive load was used to avoid capacitive mismatch (from parasitic capacitance) between HSPICE and (96). Also, the 350nm, 250nm and 180nm TSMC technologies were evaluated with 43, 35, and 28 models, respectively.

In Figure 28, box-and-whisker plots illustrate the range of agreement between the device resistance estimate and HSPICE simulation. The approximate value for device resistance is within 3% agreement to HSPICE when comparing nominal delay values (Figure 28). These findings show that the 50% delay of a transistor can be approximated by (96). Moreover, this result is agreement with a more rigorous derivation found in [8] and [130]. A similar finding has also been made in [13]. *The unique aspect of this work is the exhaustive comparisons of this linear model to more than 200 different SPICE decks, which helps to validate it use in a larger statistical simulator.*

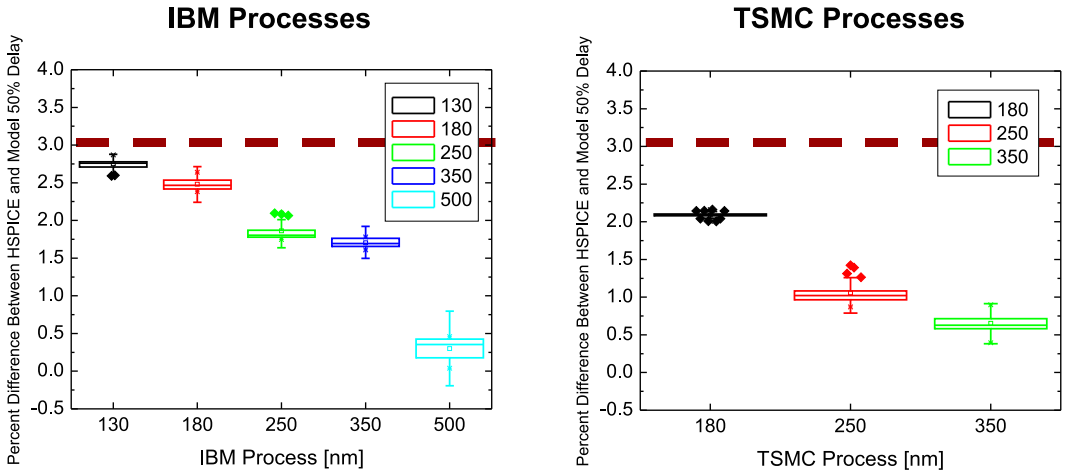

Figure 28: HSPICE 50% delay using 237 process decks (from HP and IBM combined) compared to equation (96). Closed-form estimate is found to be within 3% of HSPICE value and agrees with previous findings [13]. HSPICE 50% delay estimation is done using a 2pF capacitive load.

3.5 Wire Resistance Projections with Size Effects and LER

Using the ρ_{eff} model in (82) with 0nm LER, 6nm LER, p=0.0 and R=0.50, relative wire resistance to total circuit resistance within a single stage of a CP is shown per generation in Figure 29. Total circuit resistance is the driver resistance plus the wire resistance. Driver resistance is calculated using (96) with 75% V_{dd}. Although L_{Avg} decreases each technology generation, the non-linear dependency of wire resistivity on wire width results in an increase in the percentage of wire resistance to the total circuit resistance for future technology generations.

Figure 29 suggests that R_{int} can reach as high as 89% of the total circuit resistance for an sCore design and 69% for an mCore design by 2022 without LER. Adding 6nm LER to the interconnect increases ρ_{eff} by 29%, which maps to sCore single stage CP R_{int} increasing to 91% of total circuit resistance with mCore increasing to 74% as shown in Figure 29. As a potential solution to decrease the wire resistance, repeaters could be inserted to shorten the wire length [131] at the cost of additional power and silicon real estate.

In Table 5, single stage CP delays are calculated with no LER and are in agreement with Figure 25, where mCore single-stage delays are faster due to substantially shorter L_{Avg}'s. The significant advantage of the mCore architecture is seen at the 11nm node where as

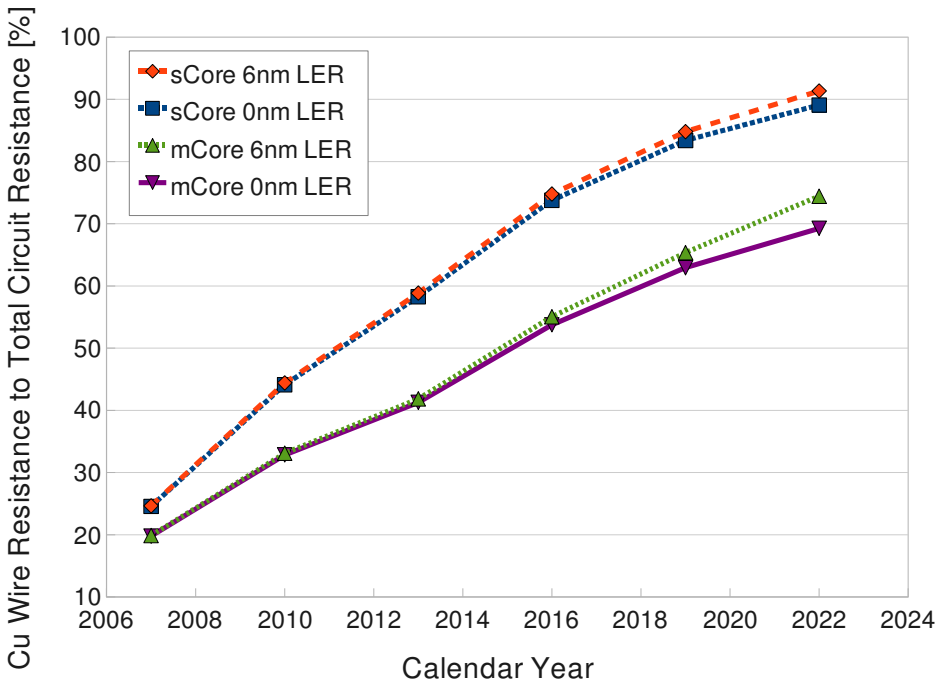

Figure 29: Interconnect resistance to total circuit resistance in a single stage of a critical path versus calendar year. The ρ_{eff} model in (82) uses the values 0nm LER, 6nm LER, p=0.0 and R=0.50. A constant number (n_{cp}) of gates in the CP with n_{cp}=8 for single core (sCore) systems and a relaxed value of n_{cp}=16 for multi-core (mCore) systems is assumed. The number of cores in an mCore system is determined by starting with 4 cores in 2007 and increasing this value 1.4X per technology node [1].

Table 5: Effective Line-Width, Number of Cores in mCore, and Nominal Single-Stage Critical Path Delays for 0nm and 6nm LER

Technology Generations			**SSCP Delays [ps]**					
Year	w_0 **[nm]**	**No. Cores**	**0nm LER**			**6nm LER**		
			sCore	mCore	↓ [%]	sCore	mCore	↓ [%]
2007	68	4	16.2	13.5	17%	16.3	13.6	17%
2010	45	11	14.6	10.2	30%	14.7	10.2	30%
2013	32	31	13.7	7.4	46%	13.9	7.5	46%
2016	22	83	13.5	5.3	61%	14.0	5.4	61%
2019	16	227	16.2	4.4	73%	17.6	4.7	73%
2022	11	623	21.3	4.1	81%	26.5	4.8	82%

much as an 82% reduction in the single stage delay is produced when switching from an sCore architecture to an mCore architecture, especially adding 6nm LER to the wire. In fact, adding 6nm LER significantly increases SSCP delay as tabulated in Table 6. Multi-core SSCP delay increased by 18.6% compared to an almost 25% increase for sCore SSCP

delay. This emphasizes the clear advantage of shorter L_{Avg} enabled by mCore architectures to reduce the impact of LER.

Table 6: SSCP Delay Increase from 0nm to 6nm LER

Technology Generations			**SSCP Delay ↑ [%]**	
Year	w_0 [nm]	No. Cores	sCore	mCore
2007	68	4	0.1%	0.1%
2010	45	11	0.4%	0.3%
2013	32	31	1.2%	0.9%
2016	22	83	3.6%	2.6%
2019	16	227	8.6%	6.3%
2022	11	623	24.6%	18.6%

Clearly, mCore designs enable shorter average wire lengths as compared to sCore designs because a 1.4X increase in the number of cores in the mCore system is assumed [1], resulting in a reduced area per core. The longer average wire lengths in the sCore system result from considering the total number of logic transistors in a single core. The mCore MPU implies all cores are identical and operate at the same frequency [1].

3.6 Core Optimization Case Study: 2022 - 11nm Node

The design of MPUs with multiple, smaller and simpler cores is the new paradigm for chip architecture. However, since core complexity increases as the number of gates per core increases and the number of gates per core directly affects L_{Avg}, there is a clear trade-off between core complexity and its impact on L_{Avg}. This design optimization can be realized should the hardware be required to handle exceedingly more complex functions per core than a smaller and simpler core. More functions per core can be interpreted, for example, as multiple threads per core, hardware-scaled video encoding/decoding or hardware supported image processing to name a few.

In this case study, the 11nm node will be critically analyzed where up to 623 cores are expected to reside on a single die. Particular attention will focus on the impact of LER and size effects on critical path frequency. The values used for this analysis are listed in Table 7. For the purposes of this case study, size effect values of p=0.0 and R=0.5 will be used as the literature has shown these to be the most pessimistic values published by industry.

Table 7: Core Optimization Case Study Parameters

Parameter	Value	Working Assumption	Source
n_{cp}	16 gates	Relaxed constraint for mCore systems	[83]
w_0	11nm	ITRS 2007 half-pitch	[1]
h_0	22nm	ITRS 2007 half-pitch × Aspect Ratio of 2	[1]
ρ_{bulk}	2.2$\mu\Omega$-cm	Effective bulk resistivity from barrier liner	[1]
p	0.0	Full specular (inelastic) scattering	[56]
R	0.5	50% Grain boundary diffusion	[56]
R_t	1590.75Ω	Assumes 2 transistors in series	[1], (95)
C_t	6.77E-16F	Assumes a fanout of 3	[1], (93)
W/L ratio	20	Typical device width to length sizing	[83]
P/N ratio	2	Typical value for pFET to nFET ratio	[83]

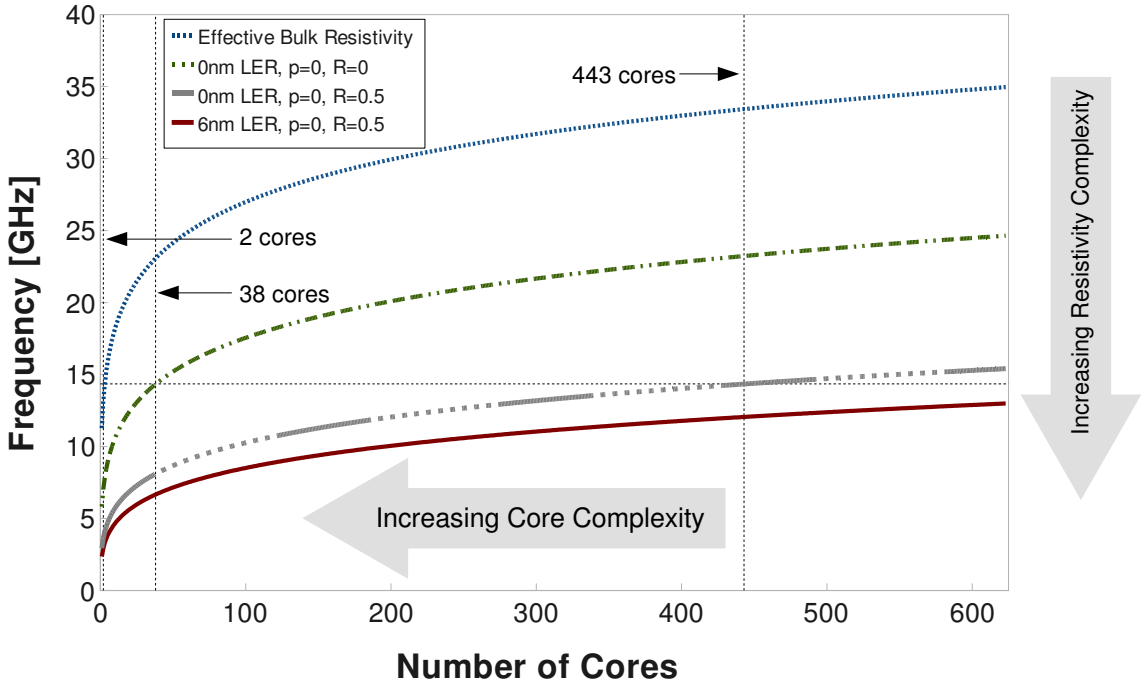

Figure 30: A plot of critical path frequency versus the number of cores. CP frequency substantially decreases as the interconnect effective resistivity complexity increases. By considering LER and size effects, there exists no minimum design point to meet the 14.343GHz on-chip clock target at the end of the roadmap for the 11nm node [1].

Figure 30 illustrates the plot of the reciprocal of the critical path delay (i.e. clock frequency) versus the number of cores for the 11nm node. Plotted are four curves assuming no LER and no size effects (ultra-fine dashed blue curve); no LER and no grain boundary

scattering (dot-dot-dash green curve); no LER, but with size effects p=0 and R=0.5 (long-dash dotted gray curve); and 6nm LER with p=0.0 and R=0.5 (solid maroon curve). The expected on-chip clock frequency for 2022 is 14.343GHz. As the number of cores decrease, individual core complexity increases. Moreover, as resistivity increases, CP frequency decreases. To optimize core size, the least amount of cores that meets the on-chip clock frequency target of 14.343GHz will be the minimum design point in Figure 30.

The ultra-fine dashed blue curve in Figure 30 shows a very large design space when only considering ρ_{bulk} for a copper interconnect. Adding sidewall scattering to the ρ_{eff} of the wire as shown in the dot-dot-dash green curve narrows the design space by having a minimum design of 38 cores on chip. To make matters worse, adding grain boundary reflectivity (R=0.5) in the gray long-dash dotted curve shrinks the design spaces further with a minimum design of 443 cores on chip. Finally, adding 6nm of LER to the size effects in the solid maroon curve closes the design space completely as the 14.343GHz target is no longer achievable. This example along with the new CP model illustrates the importance of determining effective resistivity on the system design of new multicore architectures.

3.7 Conclusions

An improved circuit-level critical path model is presented in this chapter. To develop this model, interconnect and transistor parasitics are considered and assumptions are clearly established. Interconnect parasitics are calculated using an average wire-length in the critical path. Verification of the transistor resistance is completed and is shown to be in agreement with industry data. Finally, a single stage analysis and projections for wire resistance are performed for single and multiple core architectures and show a distinct advantage of a multiple core architecture with 81% reduced single-stage delay.

CHAPTER IV

FISS: FAST INTERCONNECT STATISTICAL SIMULATOR

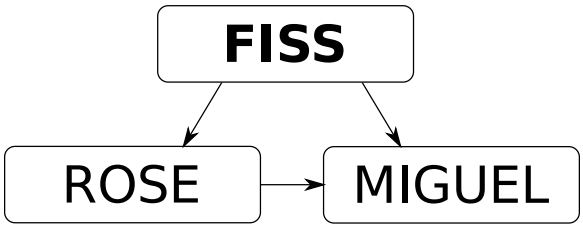

Figure 31: The Fast Interconnect Statistical Simulator (FISS) is a multi-threaded tool comprised of two statistical engines: ROSE and MIGUEL.

4.1 Introduction

In Chapter 2, a new ρ_{eff} model was derived for Task I, and the sensitivity of p and R values on ρ_{eff} was demonstrated using ITRS 2007 target values. In Chapter 3, a new critical path model was introduced for Task II with a case study of core complexity, showing the impact of the new ρ_{eff} model on design. In this chapter, Task III is fulfilled by the implementation of the Fast Interconnect Statistical Simulator (FISS). In fact, FISS facilitates the statistical analysis workflow in order to determine values for the scattering parameters p and R in Chapter 2 and to simulate the impact of interconnect process variations on the maximum critical path delay.

4.2 FISS Implementation

FISS is a highly multi-threaded tool that is comprised of two statistical engines. The engines are programmed in Java using the integrated development environment (IDE) NetBeans 6.5.1 [132] and deployed as an enterprise web application to the Sun GlassFish Enterprise Server [133]. Deploying FISS as a Java enterprise web application has three distinct advantages. First, multi-threaded programming is feasible to implement, which is useful for

statistical analysis. Second, accessibility to the application is increased since all that is required to access FISS is a web browser, ultimately making its implementation transparent. Third, results are stored into a database and may be retrieved at anytime. Since the implementation of the application server and database are beyond the scope of this work, this chapter will primarily focus on the engine algorithms implemented for FISS. The first engine is called the Regression Optimizer for Size Effects (ROSE). ROSE is used to numerically optimize the best fit of the new physical ρ_{eff} model in (82) to experimental data. The second engine is called the Metallic Interconnect Generation Utility for Experimental LER (MIGUEL). MIGUEL estimates the maximum critical path delay for any selected technology generation found in the ITRS. Optionally, any p and R value pairs and model parameters from ROSE can be ported into MIGUEL for ITRS technology generation maximum critical path delay analysis.

4.3 ROSE: Regression Optimizer for Size Effects

4.3.1 Introduction

To calibrate experimental ρ_{eff} data with the new physical model in (82), it is necessary to have a statistical engine designed to determine the possible values of p and R for best fit. Moreover, if multiple values of LER were to be also tested, multiple instances of the engine should be allowed to run concurrently to achieve improved runtime and CPU usage. With these in mind, the Regression Optimizer for Size Effects was developed. As shown in Figure 32, FISS can instantiate several instances of ROSE to calibrate the ρ_{eff} model in (82) to empirical data using different values of LER at the same time. Currently, a user may specify up to 4 LER test values. The output generated for each LER test value can be limited by setting the minimum value of best fit. In other words, ROSE will only output p and R values that yields a greater fit value than the minimum best fit value indicated by the user.

4.3.2 Workflow Description

In Figure 71, the statistical workflow is shown in greater detail. Let $\rho_{eff,i}$, w_i and h_i represent the ρ_{eff} width and height values, respectively, from physical measurement, where

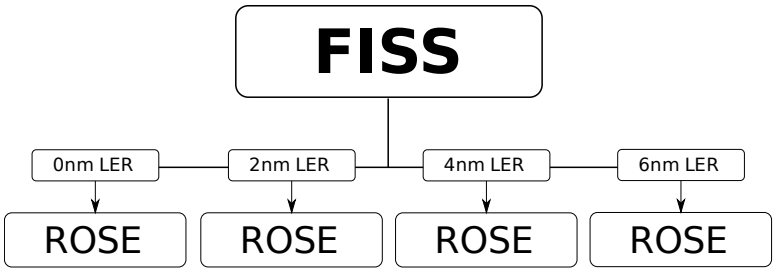

Figure 32: FISS can execute the Regression Optimizer for Size Effects (ROSE) as several individual threads to concurrently generate p and R values that best fit experimental ρ_{eff} data for the new LER ρ_{eff} model in (82).

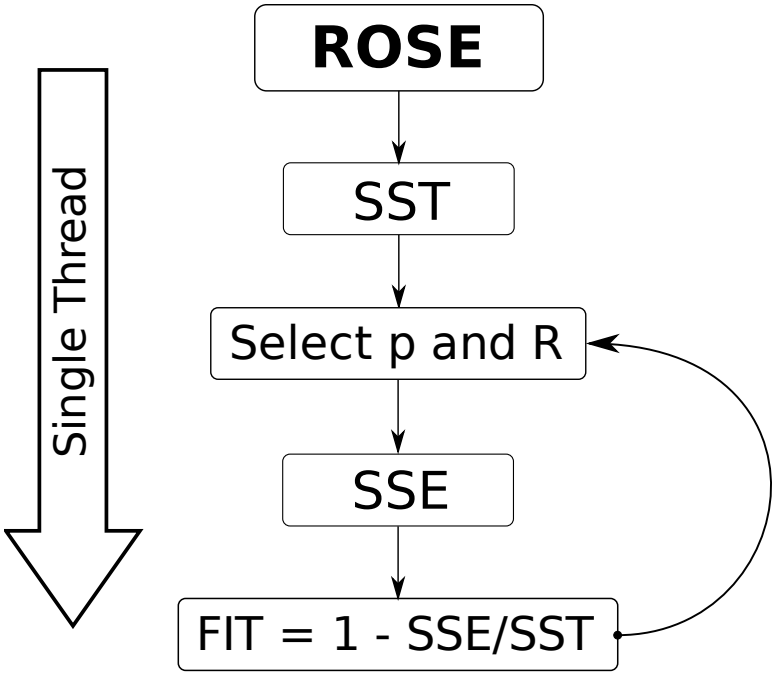

Figure 33: The ROSE engine spawns a separate thread to carry-out its statistical workflow. Values for p and R are generated and tested for best fit with the experimental data with a fixed value of LER.

$i = 1, 2, ..., n$, where n is the number of measurements in the sample. To begin, the average of the experimental ρ_{eff} data ($\overline{\rho_{eff}}$) is calculated in (97).

$$\overline{\rho_{eff}} = \frac{\sum_{i=1}^{n} \rho_{eff,i}}{n} \tag{97}$$

Next, the total sum of squares (SST) is calculated in (98) by summing the square of the difference between every experimental value $\rho_{eff,i}$ and $\overline{\rho_{eff}}$.

$$SST = \sum_{i=1}^{n} (\rho_{eff,i} - \overline{\rho_{eff}})^2 \tag{98}$$

With the SST computed, the error sum of squares (SSE) is calculated in (99) by summing the square of the difference between every experimental value $\rho_{eff,i}$ and the model found in (82), where the values of LER, p and R are evaluated. Every possible combination of p and R values between 0 and 1 at an interval of 0.01 is exhaustively evaluated and compared for best fit.

$$SSE = \sum_{i=1}^{n} \left[\rho_{eff,i} - \rho_{eff}\left(u, p, R, w_i, h_i\right)\right]^2 \tag{99}$$

Finally, the fit is calculated in (100) and resulting p and R values are returned to the user if the fit is greater than the minimum fit specified.

$$Fit = 1 - \frac{SSE}{SST} \tag{100}$$

4.4 MIGUEL: Metallic Interconnect Generation Utility for Experimental LER

4.4.1 Introduction

In Chapter 2, a new ρ_{eff} model was derived as a function of LER and size effects. The LER described by the model in (82), while it can be interpreted as a process variation, is characterized as describing the physical shape of a fabricated interconnect. Process variations for the context of this work describes the distribution of w_0 and h_0, which are the nominal width and thickness of a wire, respectively. Variation on w_0 and h_0 is denoted in terms of $\pm 3\sigma$, where $\sigma$is the standard deviation of a population that is associated with a normal distribution and mean μ. To evaluate the impact of interconnect process variations, LER and size effects on the system performance of future technology generations, a Monte Carlo (MC) statistical simulator engine is needed. Moreover, if multiple values of LER are to be tested (and to enhance runtime and CPU usage) multiple instances of the engine should be allowed to run concurrently. With these in mind, the Metallic Interconnect Generation Utility for Experimental LER (MIGUEL) was developed. Formerly written in R [134], the new multi-threaded implementation in Java improves simulation performance by 100%. As illustrated in Figure 34, FISS can spawn multiple instances of MIGUEL based on the ITRS technology node and the interconnect LER to be evaluated. In addition, any p and R values found from ROSE can be easily ported into MIGUEL, facilitating the workflow from

experimental evaluation to system performance projections of future technologies.

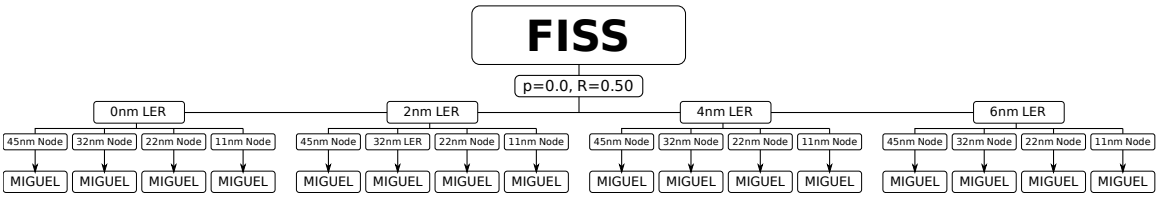

Figure 34: FISS can execute the Metallic Interconnect Generation Utility for Experimental LER (MIGUEL) as several individual threads to concurrently generate Maximum Critical Path Delay data for selected technology nodes of the ITRS.

4.4.2 Workflow Description

Using the compact models for ρ_{eff}, R_{int}, C_{int}, R_t and $t_{0.5}$ found in (82), (87), (88), (95) and (90), respectively, system performance projections can be readily obtained. The MIGUEL workflow for a single run is illustrated in Figure 35. The statistical engine begins by initializing 3 normally distributed populations of w_0. The populations represent D2D, WID-R and WID-S components of variation for w_0. Optionally, interconnect height can also be varied. Since interconnect height is strongly correlated to the unit process of CMP, one distribution is produced and used in the algorithm. The size of the population is dictated by the user. It has been found that executing 250,000 simulations per run guarantees reproducible point estimates [135] from run to run. However, the number of concurrent simulations per run is limited to the amount of memory available to the engine. On a system running Ubuntu Linux 9.04 with an Intel Core2 Quad Q9300 and 8GB of RAM, three MIGUEL engines can concurrently and adequately execute 250,000 simulations.

The D2D and WID components are assumed equal contributors to w_0, using $\pm 3\sigma_{w_0}$ 10% [85]. The total variation for w_0 is calculated using (101), where σ_{Total} is the total variation of w_0, σ_{D2D} is the D2D variation component, and σ_{WID} is the WID variation component. Both σ_{D2D} and σ_{WID} are respectively defined in (102) and (103).

$$\sigma_{Total} = \sqrt{\sigma_{D2D}^2 + \sigma_{WID}^2} \tag{101}$$

$$\sigma_{D2D}^2 = \delta \left(\sigma_{Total}\right)^2 \tag{102}$$

$$\sigma_{WID}^2 = \beta \left(\sigma_{Total}\right)^2 \tag{103}$$

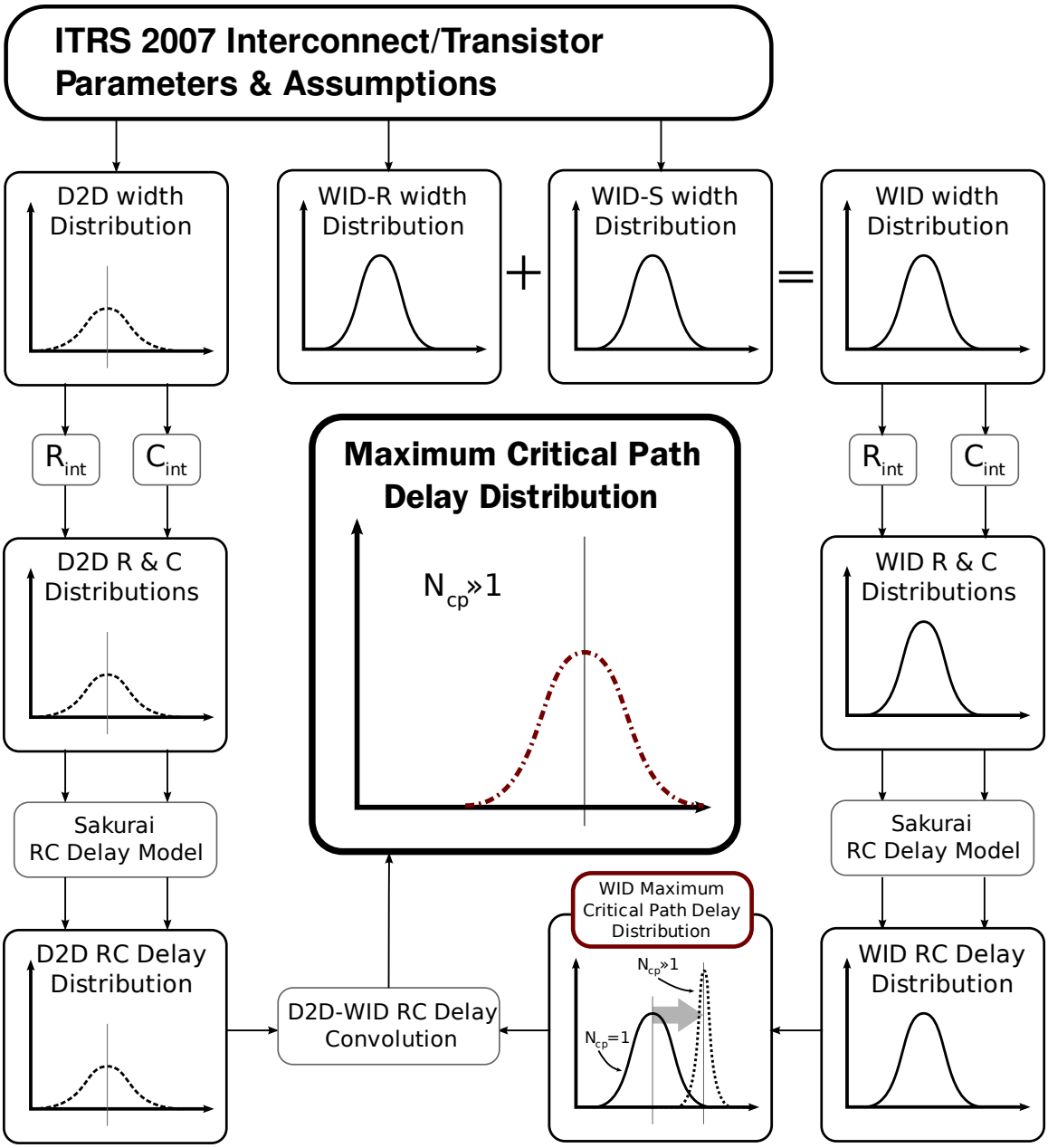

Figure 35: Monte Carlo Maximum Critical Path Delay Framework as described in [14].

The coefficients δ and β are the weighted contributions to σ_{Total}; δ and β sum to 1. Finally, the random and systematic components of WID variations are also considered equal contributors to total WID variation, yielding (104).

$$\sigma^2_{Total} = \underbrace{\frac{1}{2}\sigma^2_{Total}}_{D2D} + \underbrace{\overbrace{\frac{1}{4}\sigma^2_{Total}}^{Random} + \overbrace{\frac{1}{4}\sigma^2_{Total}}^{Systematic}}_{WID} \tag{104}$$

As illustrated in Figure 35, the D2D populations of w_0 are used to calculate R_{int} and C_{int} using the ρ_{eff} model in (82), (87) and (88) [11, 12], respectively, with the option of incorporating height variation. WID populations of w_0 are handled concurrently (with or without height variation); however, prior to calculating R_{int} and C_{int}, the two WID distributions are combined by adding the variation of one population to the other. Transistor parasitics, R_t and C_t, are calculated using (95) and (93), respectively, using values in Table 4. Once the interconnect and transistor RC values are determined, single stage delay is calculated using the 50% circuit delay model in (90) [12]. Finally, two critical path delay distributions from separate contributions of D2D and WID interconnect w_0 variations are generated.

Table 8: Assumptions for the number of cores and the number of independent CPs (N_{cp}) for each technology node

Technology Generations			
Year	w_0 **[nm]**	**No. Cores**	N_{cp}
2007	68	4	100
2010	45	11	100
2013	32	31	1000
2016	22	83	1000
2019	16	227	1000
2022	11	623	1000

From the CP delay distributions, the mean and standard deviation of a single CP are extracted separately for D2D and WID variations. The maximum CP delay distribution is then calculated using the WID population by assuming a number of statistically independent CPs (N_{cp}) on the chip, where N_{cp} values are shown in Table 8. The adjustment in N_{cp} from 32nm onward accounts for its relation to the scaling of spatially correlated regions across the die in later technologies [83]. As shown in Figure 36 from [8], as the number of independent critical paths increases, the mean delay of the distribution increases while the standard deviation decreases. In other words, as the number of slow critical paths increases, the total delay of the system increases since it is as fast as its slowest path.

Ultimately, an increase in the mean is produced in the resulting WID maximum CP delay distribution. To complete the algorithm, the WID maximum CP delay distribution

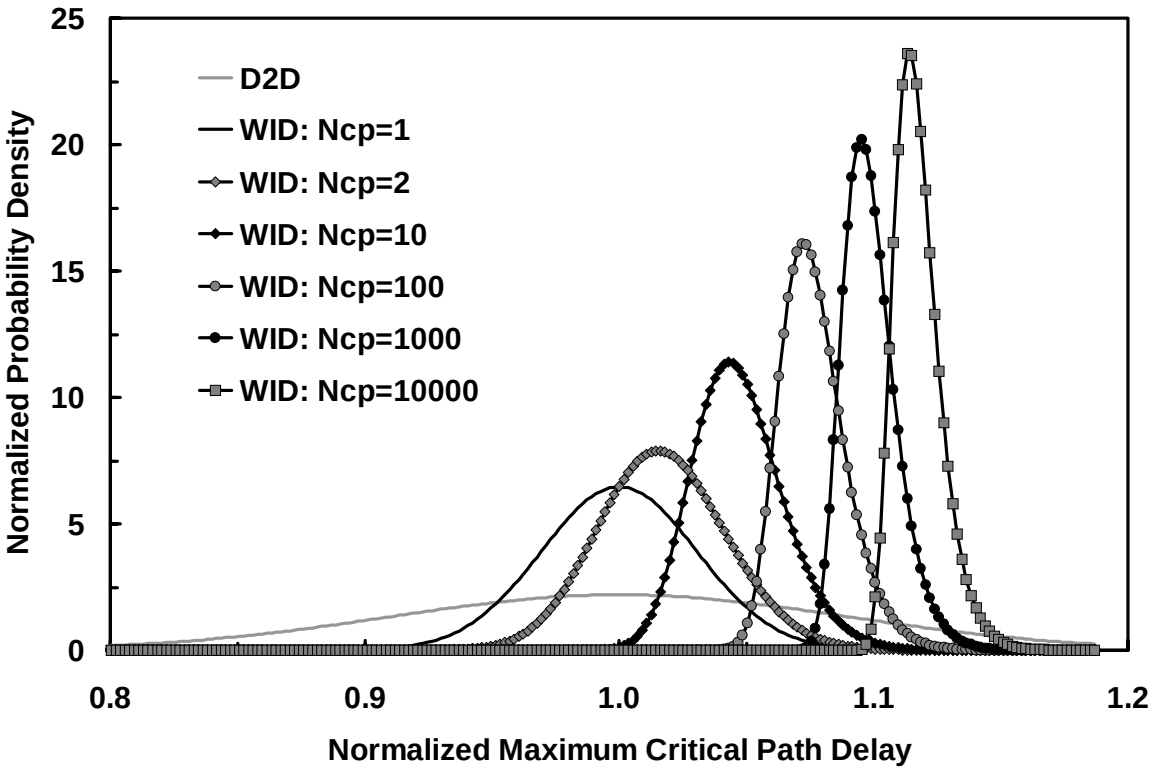

Figure 36: The within-die maximum critical path delay for varying N_{cp} [8].

is convolved with the D2D CP delay distribution to produce the final maximum CP delay distribution. The mean ($\mu_{cp,max}$) and standard deviation ($\sigma_{cp,max}$) of the maximum CP delay distribution will be analyzed in greater detail in the next section.

4.5 End of the Roadmap Projections

4.5.1 Copper Interconnects and Process Variations

Using MIGUEL, the maximum critical path delay distributions resulting from D2D and WID interconnect w_0 variations are calculated across the ITRS MPU half-pitch projections in Figure 37 and Figure 38 for both single and multi-core systems. The scattering parameters values used are p=0.0 and R=0.5. For these simulations, a 10% $\pm 3\sigma$is assumed for w_0 and h_0. D2D contributes to 50% of the w_0 variation, where WID-R and WID-S are also equal contributors of w_0 variation or 25% each. In Figure 37 and Figure 38, the relative shift or mean increase of the $\mu_{cp,max}$ and the relative size of $\sigma_{cp,max}$ to $\mu_{cp,max}$ are plotted, respectively.

Until 2016 (22nm), w_0 variation dominates the LER variation because the LER amplitudes are substantially smaller than the nominal w_0. From 2016 (22nm) to 2022 (11nm), LER amplitudes start to become a significant percentage (14-27%) of nominal w_0, thus increasing the target ρ_{eff}. This trend exacerbates the size-effects, leading to an increase in the maximum critical path delay mean ($\mu_{cp,max}$) and standard deviation ($\sigma_{cp,max}$) for both sCore and mCore systems.

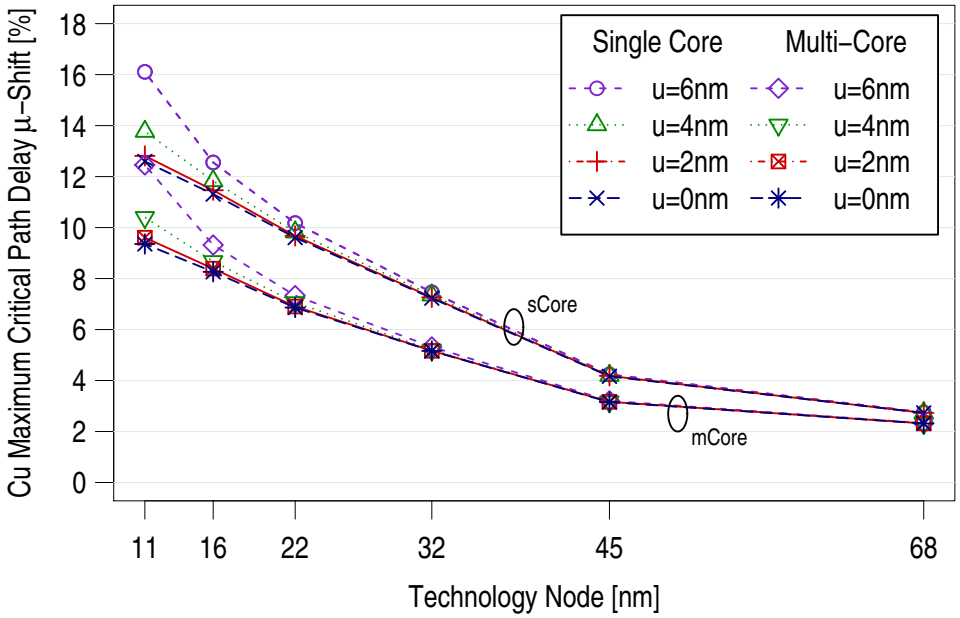

Figure 37: Copper Maximum CP delay mean increase versus ITRS MPU half-pitch for single and multi-core systems for a range of LER amplitudes.

Prominent differences between sCore and mCore systems in the $\mu_{cp,max}$ increase and $3\sigma_{cp,max}$ are revealed in Figure 37 and Figure 38. With 6nm LER at a 11nm half-pitch, simulation results indicate a 23% reduction in both the $\mu_{cp,max}$ increase and $3\sigma_{cp,max}$ from the sCore system to the mCore system. The benefits of the mCore design directly correspond to the reduction in L_{Avg} relative to the sCore system. In short, mCore systems enable shorter wires than sCore systems. At 2022, the mCore L_{Avg} value is 72% shorter than the sCore L_{Avg} value (Fig. 4), and consequently, the mCore single-stage delay is reduced by 81% (Table 5). As a result, mCore interconnect resistance is considerably lower than sCore, thus mitigating the overall impact of interconnect process variations and size-effects on the maximum CP delay distribution as evident in Figure 37 and Figure 38. In summary, our

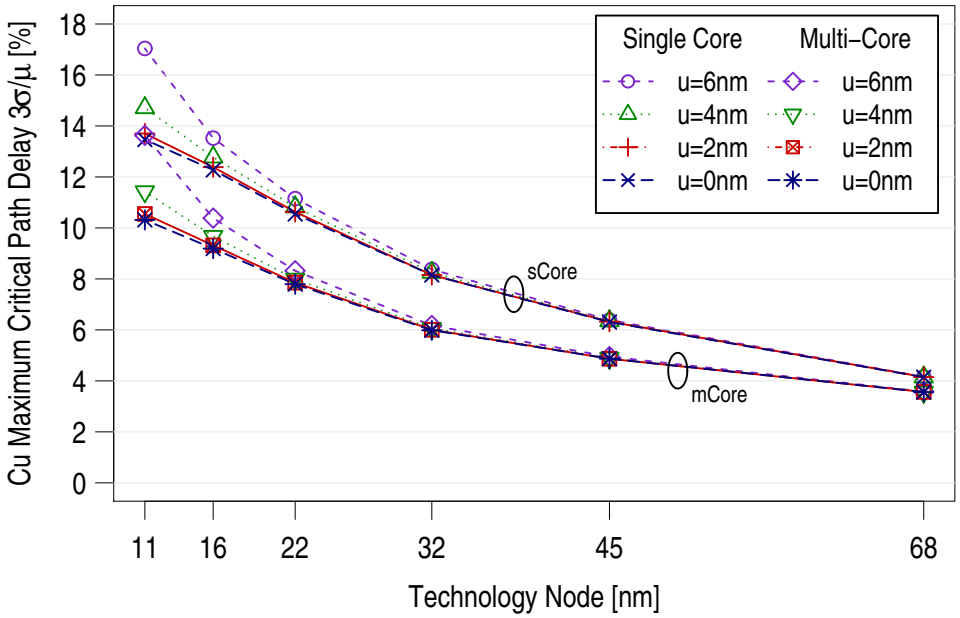

Figure 38: Copper Maximum CP delay 3σ versus ITRS MPU half-pitch for single and multi-core systems for a range of LER amplitudes.

analysis suggests that mCore systems are more tolerant to interconnect process variations than sCore systems due to the inherent short-wire architecture in mCore designs.

4.5.2 Aluminum Interconnects and Process Variations

Materials with a shorter mean free path than Cu and comparable ρ_{bulk} may extend the benefit of short wire architectures [7,53] as shown in Figure 7. For the purpose of this work, Al is chosen as a case study example using MIGUEL and applying the same scattering, w_0 variation and h_0 variation values. Aluminum has a mean free path λ_{Al}=14nm in bulk at 300K with ρ_{bulk}=2.65$\mu\Omega$-cm. Assuming scattering parameters (R and p) and a range of LER amplitudes, a normalized study for comparison can be done for Al. In fact, aluminum with has been investigated for dimensions smaller than λ_{Cu} [5,7,52,53] as size effects appear to be mitigated due to a smaller λ.

Figure 39 and Figure 40 describe similar trends between a long-wire architecture (sCore) versus a short-wire architecture (mCore) as in Figure 37 and Figure 38, respectively. Because $\lambda_{Al} < \lambda_{Cu}$ and ρ_{bulk} is comparable for scaling physical dimensions, there is a significant reduction from size effect impact when comparing the respective figures. This reduction is

noticeable by comparing the absolute values of a mCore Cu $\mu_{cp,max}$ to that of a mCore Al $\mu_{cp,max}$ for 0nm LER and 6nm LER in Table 9, there is as much as a 42% decrease in the $\mu_{cp,max}$at the 11nm node.

Table 9: Percent decrease for absolute values of $\mu_{cp,max}$ and $3\sigma_{cp,max}$ when changing from Cu to Al with corresponding LER for mCore systems.

Technology Generations			**LER=0nm**		**LER=6nm**	
Year	w_0 [nm]	No. Cores	$\mu_{cp,max}$	$3\sigma_{cp,max}$	$\mu_{cp,max}$	$3\sigma_{cp,max}$
2007	68	4	5%	16%	4%	14%
2010	45	11	12%	32%	9%	31%
2013	32	31	19%	38%	14%	36%
2016	22	83	28%	43%	22%	43%
2019	16	227	36%	47%	28%	47%
2022	11	623	42%	50%	36%	51%

Likewise for absolute values of a mCore Cu $3\sigma_{cp,max}$ to that of a mCore Al $3\sigma_{cp,max}$ for 0nm LER and 6nm LER in Table 9, there is as much as a 51% decrease in the $3\sigma_{cp,max}$ by the end of the roadmap. In other words, a short mean free path of λ_{Al}=14nm translates to a dramatic reduction in delay (increase in performance) with reduced impact of size effects from LER and w_0 variation. Aluminum is in practice its own worst enemy with its affinity to react with its surrounding and self-passivate as discussed in [5] and [6]. As a result, its comparable effective resistivity to Cu is lost.

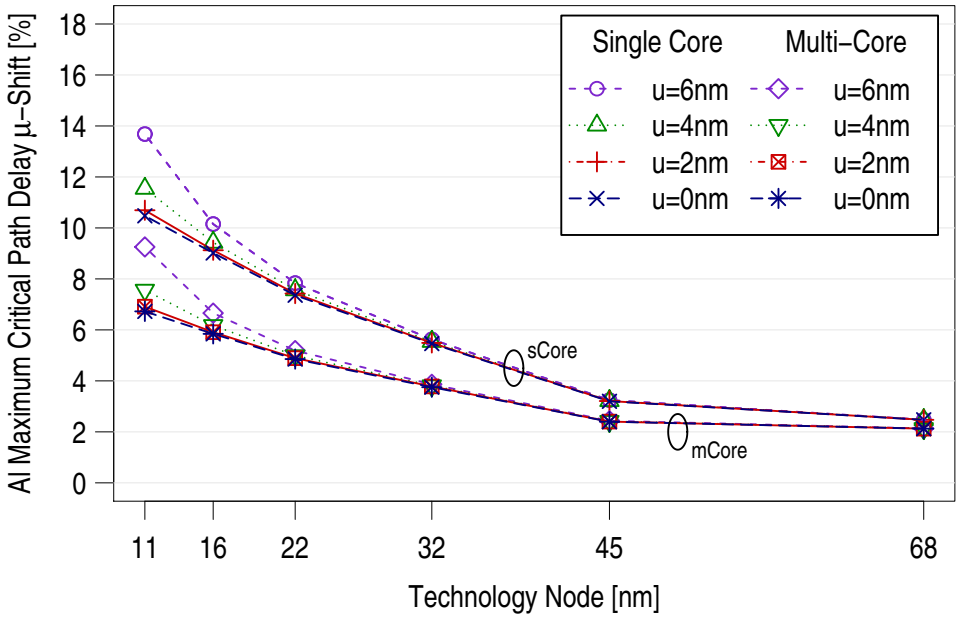

Figure 39: Aluminum Maximum CP delay mean increase versus ITRS MPU half-pitch for single and multi-core systems for a range of LER amplitudes.

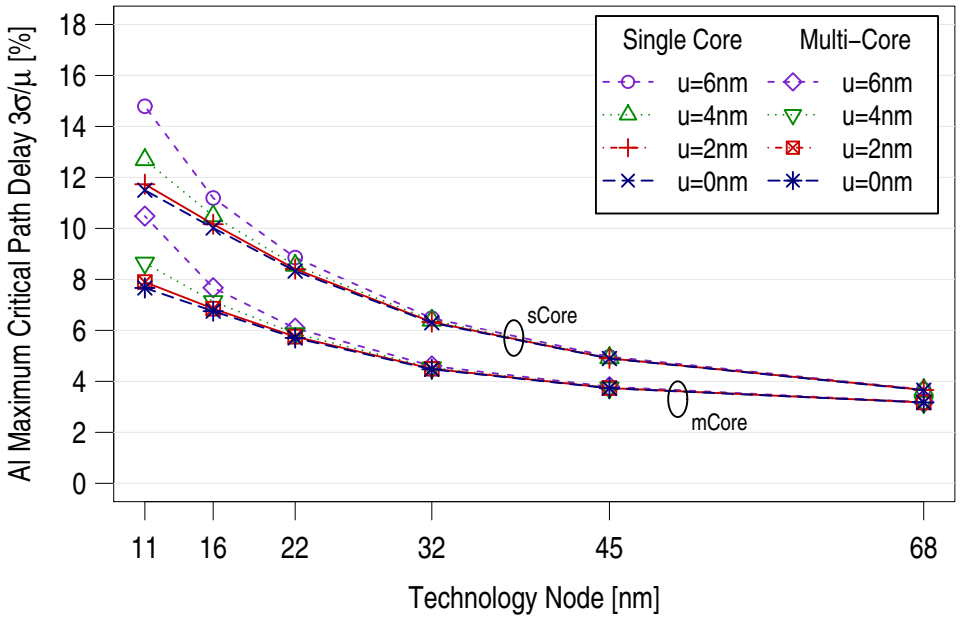

Figure 40: Aluminum Maximum CP delay 3σ versus ITRS MPU half-pitch for single and multi-core systems for a range of LER amplitudes.

4.6 Conclusions

In this chapter, the Fast Interconnect Statistical Simulator (FISS) was developed. FISS is composed of two statistical engines. The first statistical engine is the Regression Optimizer for Size Effects (ROSE), which is used to numerically calibrate experimental ρ_{eff} measurements to the new ρ_{eff} model in (82). The second statistical engine is the Metallic Interconnect Generation Utility for Experimental LER (MIGUEL), which is used to make performance projections for future architectures from the impact of interconnect process variations. Using MIGUEL, it is found that multiple core architectures are more tolerant to process variations by way of their inherently shorter wires. To extend this tolerance by changing the material to that with a shorter mean free path than λ_{Cu}, a performance gain seen with a 42% $\mu_{cp,max}$decrease and 51% narrower CP distribution ($3\sigma_{cp,max}$) becomes readily apparent.

CHAPTER V

NANO-INTERCONNECT PROCESSING AND FABRICATION

5.1 Introduction

Task I derived a new closed-form ρ_{eff} model for metallic interconnects as a function of line-edge roughness (LER) and size effects. This task showed that careful selection of scattering parameters can have significant impact on projections especially when the amplitude of LER is comparable to the nominal interconnect line-width. Using the new model from Task I, Task II established a new critical path (CP) model that included interconnect RC parasitics as opposed to the former model in [8] where only interconnect capacitance is considered. Using the new CP model, the benefit of a short-wire architecture, such as a multi-core design, was demonstrated. Moreover, a case study on the 11nm node elucidated the important trade-off between core complexity and core clock frequency. It noted that if LER and size-effects are ignored for average wire lengths, MPU design windows could be completely off target. In Chapter 4, Task III was completed by the design and implementation of FISS, the Fast Interconnect Statistical Simulator, which is comprised of two statistical engines: the Regression Optimizer for Size Effects (ROSE) and the Metallic Interconnect Generation Utility for LER (MIGUEL). Simulations indicate that using a material with a $\lambda<\lambda_{Cu}$ may offer increased the tolerance to size effects impact that manifest at the sub-40nm for Cu. To explore this idea further, the design, process development and fabrication of metallic interconnects at the 22nm technology node are required for empirical resistivity measurement and comparison.

In this chapter, Task IV develops a fabrication process to realize interconnect test structures that will be used to calibrate the new model in Task I. To begin, the set of tools needed for interconnect fabrication must be established along with the steps needed for

fabrication. Various test structures must be explored and should consider processing limitations. Next, process optimization is required to control parameters such as grain growth, thin film deposition and lift-off.

5.2 Tools Required for Fabrication and Metrology

At the Georgia Institute of Technology Nanoelectronics Research Center, the facility features key nano-enabling tools that make nano-interconnect processing possible. Namely, the major tools for fabrication are the EBL CEE 100CB Spinner, JEOL JBX-9300FS E-Beam Lithography (EBL) Tool in Figure 41 and the CVC E-Beam 1 Evaporator (CVC1) in Figure 42. Tools used in metrology are the Nanospec Refractometer for resist and oxide thickness measurements; the Veeco Atomic Force Microscope (AFM) in Figure 43 for step height measurements; and the Carl Zeiss Ultra 60 SEM in Figure 44 for top-view lateral measurements.

Figure 41: The JEOL JBX-9300FS E-Beam Lithography (EBL) Tool used for pattern writing.

Figure 42: The CVC E-Beam 1 Evaporator used for metal deposition.

Figure 43: The Veeco AFM used for step height measurements.

Figure 44: Carl Zeiss Ultra 60 SEM used for top-view lateral measurement.

5.3 Test Structure Design

The test structure designed for resistivity measurement is a two point probe (2PP) configuration. Since the wire resistance is expected to be several orders of magnitude greater than the contact resistance, the 2PP configuration is able to estimate the wire resistivity adequately. To avoid Schottky resistance issues as in [136], the structure will be monolithic. To facilitate this requirement, the contact pads and wire will be composed of the same metal and fabricated in one step.

Several test structure configurations were considered. Two structures rendered working samples. Illustrated in Figure 45 and 46, the 2PP configuration will consist of a 5μm or 530μm long interconnect between two pads, respectively. The short 5μm wire has shown to have higher yield in fabrication for narrower line-widths. The elimination of corners such as those found in the serpentine structure in Figure 46 prevented complications arising from weak points in the structure for narrower lines. Similar findings has also been reported in [89].

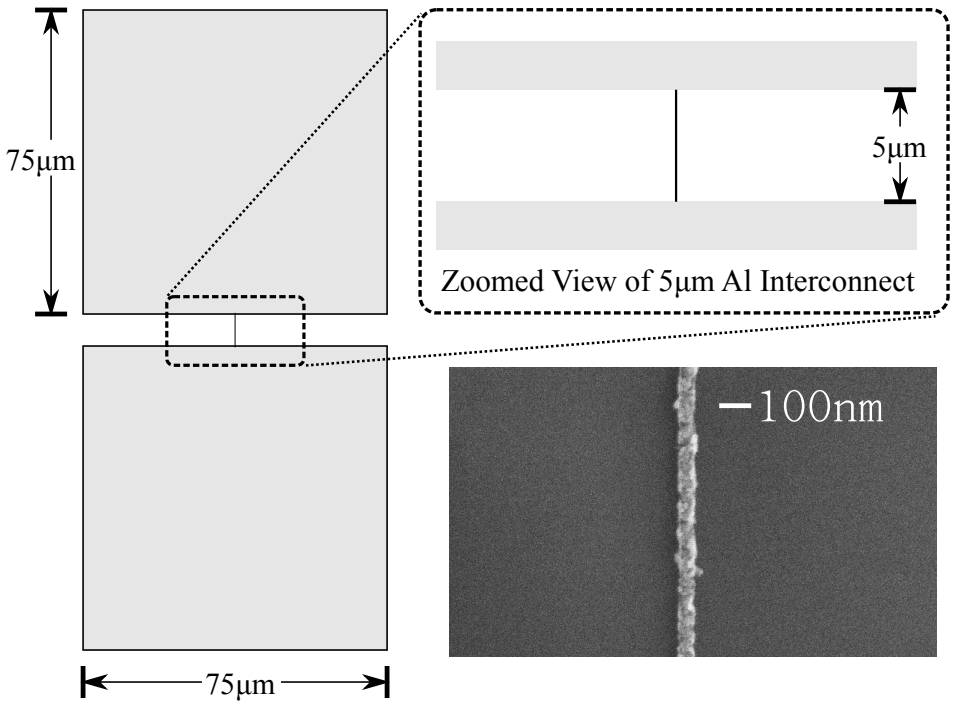

Figure 45: Two Point Probe configuration with a 5μm interconnect. Both the contact pads and interconnect are fabricated using a lift-off process. Inset: an SEM graph of a realized 50nm wide Al interconnect test structure.

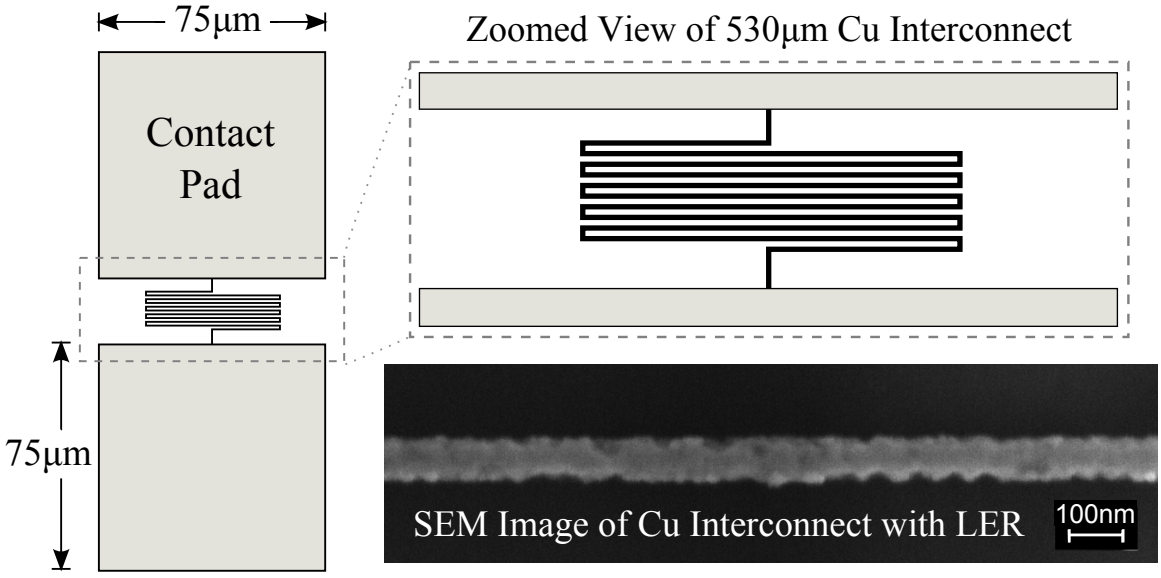

Figure 46: Two Point Probe configuration with a 530μm serpentine interconnect. Both the contact pads and interconnect are fabricated using a lift-off process. Inset: an SEM graph of a realized Cu interconnect with natural LER.

5.4 Fabrication

The fabrication of nano-interconnects are discussed in this section. Necessary steps are required to produce a testable 2PP structure with desired CD. Careful attention to resist thickness, e-beam exposure and metal deposition helped to optimize the process flow.

5.4.1 Substrate Preparation

To fabricate nano-interconnects, a substrate is needed. For the purpose of this work, 4 inch test grade, single-side polish, 400μm thick Si wafers are used (Figure 47). Since the electrical properties of the Si are not exploited, doping information is irrelevant. Using the Tystar Polysilicon Furnace, SiO_2 (shown as light blue in Figure 48) is thermally grown on the substrate, shielding any electrical contact to the semiconductor. Using the Nanospec Refractometer, oxide thickness measured 830nm uniformly across the wafer.

Figure 47: The nano-interconnect process begins with a 4 inch bare, test grade, single-side polish Si wafer that is approximately 400μm thick.

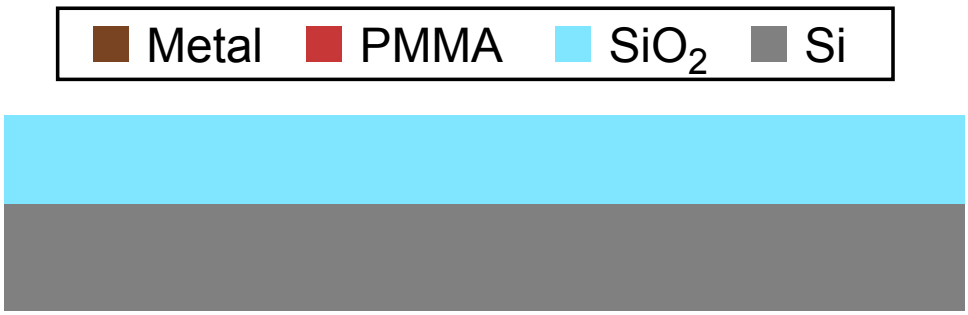

Figure 48: SiO_2 is thermally grown to a thickness of 830nm using the Tystar Polysilicon Furnace.

The remaining step in substrate preparation is the application of polymethyl methacrylate (PMMA) using the EBL CEE 100CB Spinner. For this work, it is important to note

the thickness of the resist. For proper liftoff to occur, the resist should be at least twice the height of the total metal deposition. After applying 950 PMMA A2 to the center of the wafer (enough to cover about 2/3 of the wafer area), the wafer is spun for 62s at 2000RPM with a 1000RPM/s ramp up. The wafer is then placed on a hotplate at 180°C for 90s to evaporate the anisole solvent to cure the resist. The resulting thickness of the PMMA measures approximately 85nm using the Nanospec Refractometer and is consistent with AFM step height measurements (Figure 49).

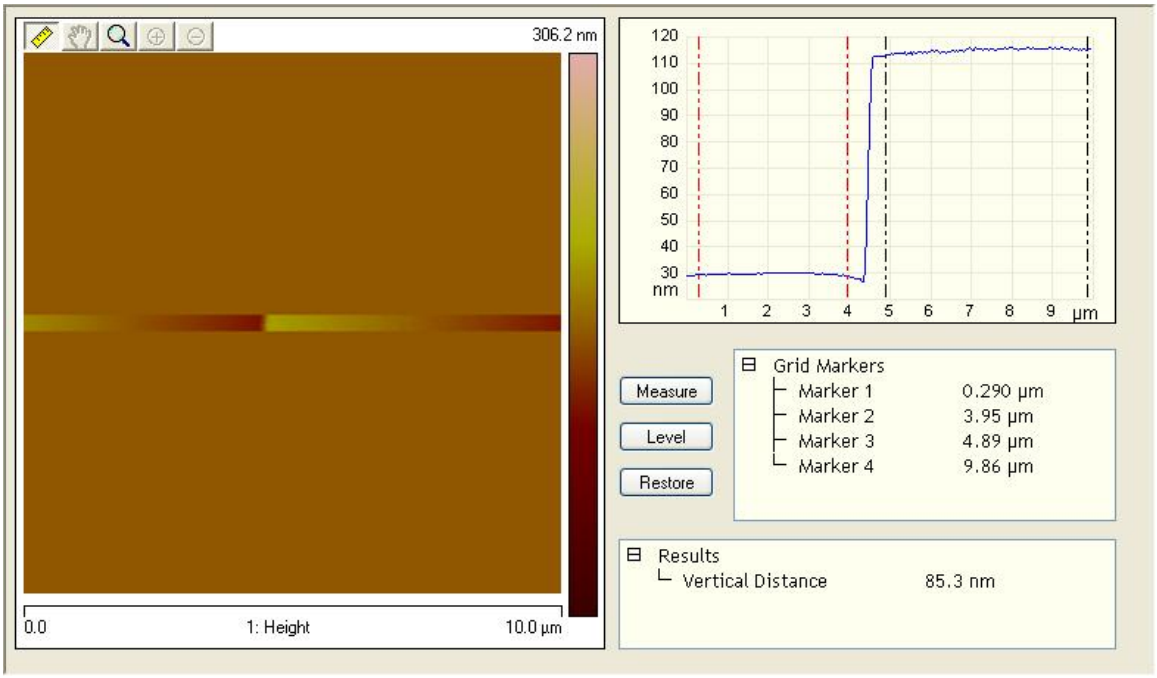

Figure 49: A sample step height measurement for PMMA resist using the Veeco AFM. Step height measurements are consistent with Nanospec Refractometer measurements for resist thickness.

5.4.2 Pattern Writing and Development

In the previous subsection, the substrate was prepared with a thermally grown insulator and spin coated with PMMA as shown in Figure 50. PMMA is a positive resist that is sensitive to e-beam radiation and has been shown to have excellent resolution down to 20nm [137]. When exposed, the PMMA chemically alters and becomes readily soluble to a developer solution. To reduce cost and waste, the wafer is cleaved into approximately $1cm^2$

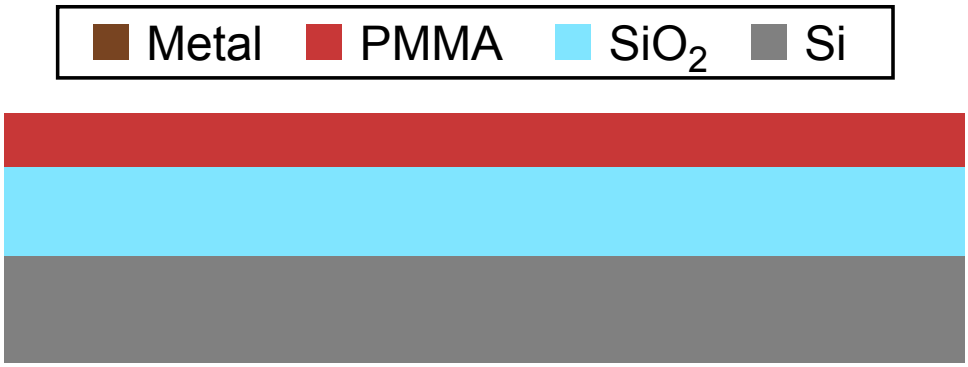

Figure 50: Positive photoresist 950 polymethyl methacrylate (PMMA) A2 is spun on to a thickness of approximately 80nm by spinning the wafer at 2000RPM for 62s with a 1000RPM/s ramp up.

pieces. These pieces or chips are carefully placed into the piece cassette of the JEOL JBX-9300FS for pattern writing. Pattern writing is depicted in Figure 51, where the e-beam is represented in yellow with down arrowheads and the exposed resist in pink. Prior to every exposure, JEOL JBX-9300FS is calibrated. Base dose for the pattern writing of contact pads and wire patterns are $550\mu C/cm^2$ and $1000\mu C/cm^2$, respectively.

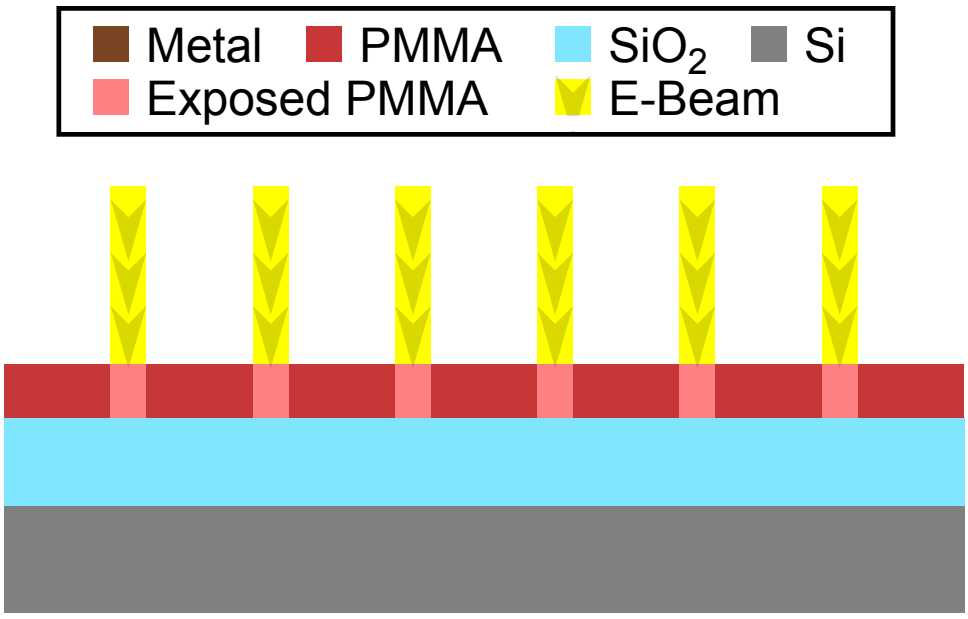

Figure 51: A pattern is written to the resist using the JEOL JBX-9300FS by applying a dose of energy to a desired area. The exposed portions of the resist are then chemically altered and will dissolve readily in a developer.

Once the exposure is complete, the chip is removed from the cassette and is ready for

development. A fresh developer of 2:1 IPA:H_2O is created prior to every development. The chip is submerged for 12s and dried immediately using an N_2 gun atop of absorbent tex-wipes. With the pattern developed, exposing the SiO_2 beneath, the chip (Figure 52) is now ready for metal deposition.

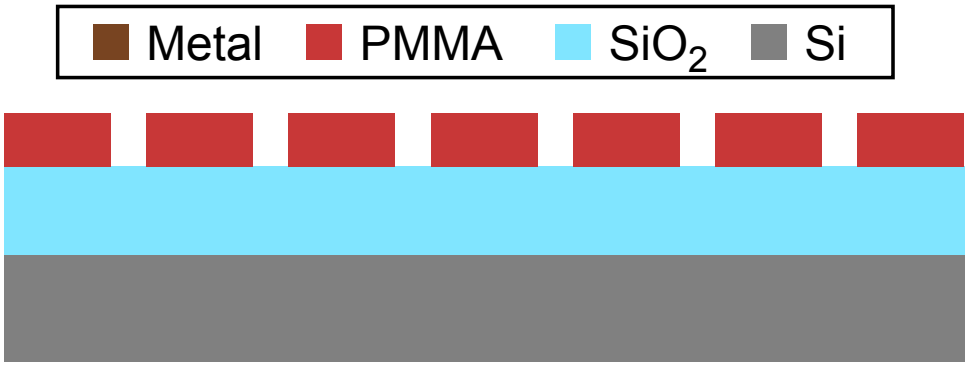

Figure 52: By using a developer composed of 2:1 IPA:H_2O, the sample is submerged for 12s and dried using N_2. Exposed parts of the resist is immediately dissolved. The short development time has shown good reproducible critical dimensions.

5.4.3 Metal Deposition

Metal deposition is performed using the CVC E-Beam 1 Evaporator. Careful consideration to the chamber vacuum, the distance from the source crucible to the chip, position of the chip on the sample plate holder and the deposition rate must be performed to ensure small uniform grain growth. Deposition is started once the chamber vacuum falls near 1.0μTorr. To achieve this vacuum, the chamber must remain in pumpdown for approximately 1.5hrs. To accelerate pumpdown or to absorb any remaining moisture or air in the chamber, a Ti burnout can be performed starting at $\sim$6μTorr, by setting the deposition rate to 3.0Å/s at a deposition of 2000kÅ with the shutter closed.

To decrease the amount of radiation seen by the chip during deposition, the sample holder is raised further from the source crucible. This is done using the rotating platform especially made for the evaporator as shown in Figure 53. Finally to keep metallic grain sizes small, an aluminum blocked is placed on the backside of the sample holder to serve as a heat sink, and the deposition rate is dialed in as 0.2Å/s, 1Å/s and 0.5Å/s for Cr, Cu and Al, respectively.

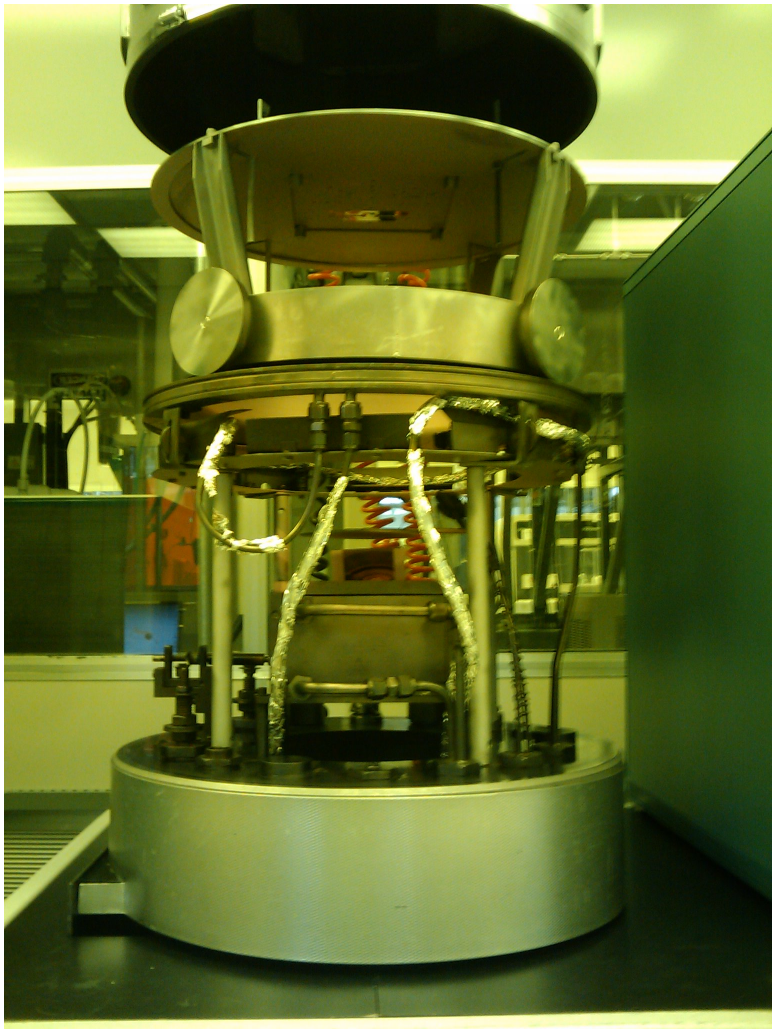

Figure 53: To decrease the amount of radiation seen by the chip during deposition, the sample holder is raised using the rotating platform especially made for the evaporator.

To adhere Cu to SiO_2, a thin adhesion layer (seed layer) of Cr is first needed. Cr was chosen since it has mean free path of roughly 32nm [138] and (38nm when alloyed with Cu [139]) with a bulk resistivity of 12.5$\mu\Omega$-cm [140]. Based on the orientation of the Cr crystal, bulk resistivity can be as low as 10.8$\mu\Omega$-cm [141]. To minimize the impact of CrCu alloying on resistivity [139], a very thin seed layer is deposited. Optimization of the seed layer allows for less than a 1nm deposition of Cr at a rate of 0.2Å/s. Copper can then be deposited at rate of 1.0Å/s at a maximum deposition of 200nm. Since the height of the sample is increased, the actual deposition of Cu is roughly a quarter of the dialed-in deposition of 200nm to realize a $\sim$40nm Cu thin film. For aluminum, no seed layer is

needed. A typical deposition of 150nm will yield a ∼40nm thin film of Al at 0.5Å/s. Once deposition is complete, a cool down time of 15 minutes is required to guarantee extended crucible life and minimal surface oxidation.

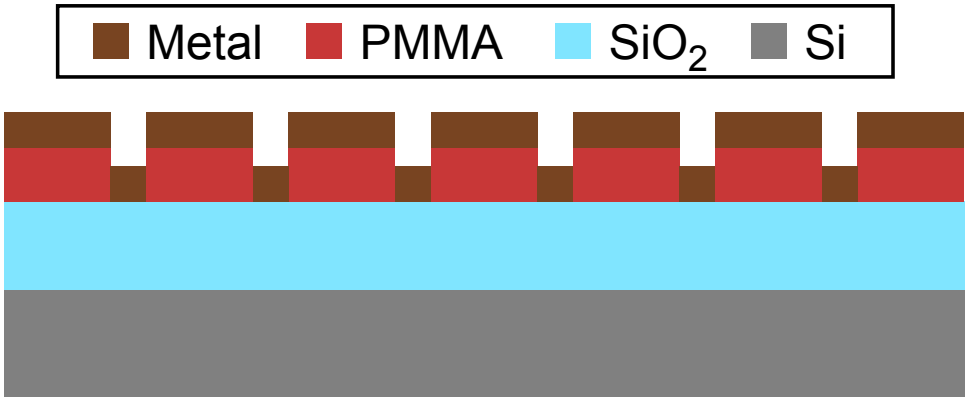

Figure 54: Approximately 1nm Cr and 40nm of Cu is deposited using the CVC E-Beam 1 Evaporator. Cr is needed as an adhesion layer for Cu to SiO_2. Al does not require a seed layer and can be deposited directly onto SiO_2.

5.4.4 Metal Lift-off

In order for metal lift-off to be successful, the metal thickness should not exceed half the height of the resist [142]. After appropriate cool down, the chip is removed from the sample holder and placed into a pre-heated beaker of 1165 at 85°C anywhere from 10min to 1hr with no mechanical agitation. Excess Cu lifts off readily and should be visibly floating in the thermal convection currents in the 1165. Aluminum, however, does not lift-off in the same fashion. A special rinse will be described shortly to remove the excess metal. Depending on the hot plate used, raising the 1165 stripper to 85°C may require setting the temperature to as much as 150°C. A digital thermometer should be used to monitor the temperature of the solvent since the flash point of 1165 is at 88°C in a closed-cup. No more than 60mL of 1165 should be needed for lift-off. A second and third soak (∼5-10min each) in two other pre-heated beakers are used to fully dissolve the resist.

After the hot 1165 bathes, the chip is carefully removed and gently rinsed in using AMI (acetone, methanol and isopropyl alcohol (IPA)). For Cu, a gentle dip in a bath of acetone, methanol and IPA is used (Figure 57). Since Al tends stick better to the surface, a gentle

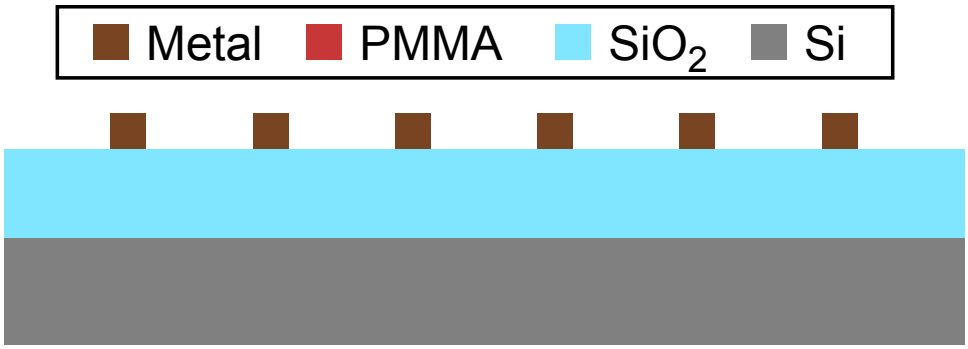

Figure 55: The sample is submerged in a bath of hot 1165 at 85°C to dissolve the PMMA, lifting off the excess metal.

Figure 56: A sample with Cu submerged in a bath of hot 1165 at 85°C. Lift-off has already started around the edges of the deposition.

flow of acetone and IPA is ran over the sample using their respective rinse bottles. To achieve an even flow of solvent using the acetone and IPA rinse bottles, it is important to use bottles that are full or near full. Direct flow to the chip and patterned area should be avoided as much as possible so as not to damage the delicate wires. Finally, the sample is dried atop of tex-wipes using an N_2 gun.

Figure 57: Samples with Cu are dipped in a bath of acetone, methanol and IPA. Samples with Al must be rinsed directly to remove the metal.

5.5 The Challenges of Nano-Interconnect Fabrication

The nano-interconnect fabrication is wrought with challenges. Among each of the process steps described in the previous section looms variability. Moreover, higher level issues such as equipment maintenance/downtime, equipment scheduling and contamination were problematic in generating interconnects for test. In this section, the challenges in each of the process steps are described in greater detail to appreciate the painstaking task of the experimental portion of this body of work.

5.5.1 EBL CEE 100CB Spinner: Resist Thickness

The challenge in substrate preparation fell to spin coating the wafer with resist. Using 950 PMMA A2, the wafer is for 62s at 2000RPM with a 1000RPM/s ramp up. As noted in the

fabrication this should yield an approximate thickness of 85nm for most cases. Using the Nanospec, a set of wafers spun in the described fashion would also yield thickness ranging from 75nm to 110nm. In other words, a single wafer would uniformly have 75nm thick resist, 85nm thick resist, 110nm thick resist, etc. To compound the issue of substrate preparation, having variability in the thickness required a re-characterization of e-beam exposure. This means that when a wafer with 75nm thick resist was used up, switching to an new wafer with 100nm thick resist would have to be tested for consistency with its predecessor.

5.5.2 JEOL JBX-9300FS E-Beam Lithography Tool: Critical Dimension Reproducibility

The narrowest, yet untestable, metallic interconnect produced using e-beam lithography is roughly 20nm as shown in Figure 58. This can be achieved by having a resist thickness of ∼45-50nm and using a single pass exposure set at an optimal dose without the writing of contact pads. The optimal dose is usually found by creating a design that draws the same line-with using different dosing levels, realizing the structure with metalization and performing lift-off. However, once larger structures such as contact pads are placed in the vicinity of the wire pattern, the back scattering electrons from the pad exposure increase the line-width significantly from secondary exposure.

Because of backscattering, line-width optimization turned to a more time consuming approach by pattern writing a complete test structure (contact pads and interconnect) and by increasing the dose of the wire. Compounding the issue, since proper metal lift-off requires the resist to be at least double of the deposited metal, it was difficult to produce such fine dimensions with thicker resist. Finally, since PMMA tends to charge easily under the SEM (which severely distorts the image), the only way to view the narrow line-widths is by completing the metalization and lift-off steps completely. Obviously more time consuming, executing the full process gave options for refinement along the way.

5.5.3 CVC E-Beam 1 Evaporator: Metal Deposition

Metal deposition using the CVC E-Beam 1 Evaporator also has many challenges. Deposition control, grain size control and chamber pressure were the primary challenges when

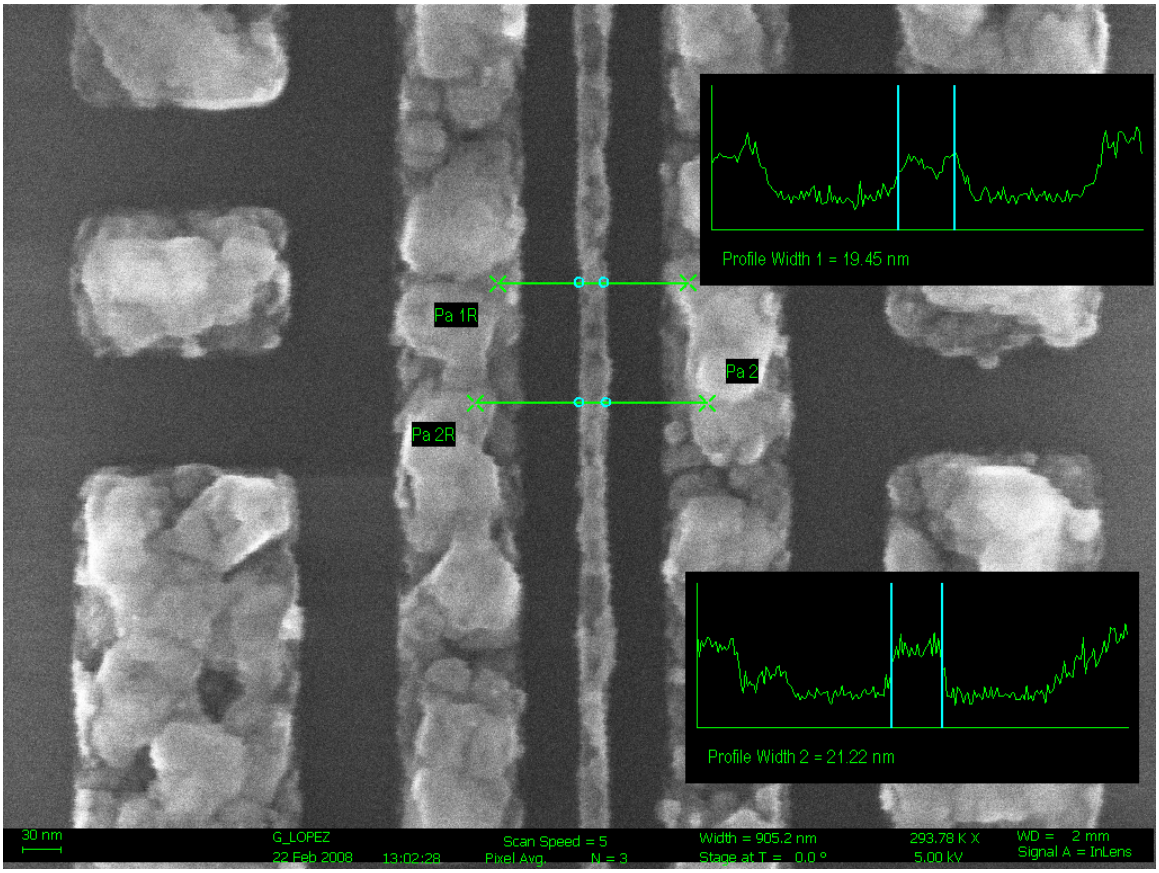

Figure 58: Minimum line-widths achieved were roughly 20nm as shown above in the contrast curve measurements of the Al interconnect. Because of significant charging of PMMA, metallic lines had to be fabricated to see the minimum line-width that was patterned. The surface roughness was enhance by controlling grain growth and shrinking the grain size.

performing metal deposition and to achieve good lift-off. This subsection discusses these challenges in detail to appreciate the level of optimization used for this particular tool.

5.5.3.1 Deposition Rate Stabilization

The CVC 1 does not start depositing metal once the deposition rate is stable. In fact, deposition stabilization often occurs for many cleanroom users during the deposition phase, which adds uncertainty to process. To control the deposition rate, the shutter must be controlled manually using the control panel in Figure 59. For instance, the deposition of Cr and Cu is done by manually opening the shutter once the desired deposition rate is achieved. To achieve the desired deposition rate of 0.2Å/s for an approximate 1nm deposition of Cr, the Zero Thickness button must be held down until the deposition rate is achieved. If

not, the *dialed-in* 1nm deposition would be achieved prior to releasing the shutter, thus shutting off the beam. Deposition control for Cu is handled in a similar manner with the exception of holding down the Zero Thickness button. Once the deposition rate is achieved, the deposition is zeroed and the shutter is released at the same time. With that said, it is always a good idea to check the shutter functionality prior to pumpdown. Moreover, it is important to check the Cr and Cu crucibles for any contaminants.

Figure 59: The deposition of Al, Cr and Cu is done by manually opening the shutter once the desired deposition rate is achieved. The mode must be set to manual (MAN) with the shutter set to CLOSE. The power must always be set to ON.

5.5.3.2 Grain Size Control

The ability to control grain growth was also explored for this work. Typically, the smaller the grains, the smoother the surface of the thin film with increased height uniformity. Between Cu and Al, Al required finer optimization for grain growth. In Figures 60 and 61, there are visible differences between grain structures. Both images were takes at 50X magnification using the Zeiss SEM. The thin film with larger grain sizes have an average radii of 50nm as compared to the thin film with an average radii of 20nm. Grain growth for Al was determined to be largely chamber pressure dependent with a fixed deposition

rate of 0.5Å/s. It was determined that the chamber must be in a range of 1.0-2.4μTorr to achieve reproducible results. As a result, improvement to the surface roughness is evident when comparing Figure 58 to Figure 62.

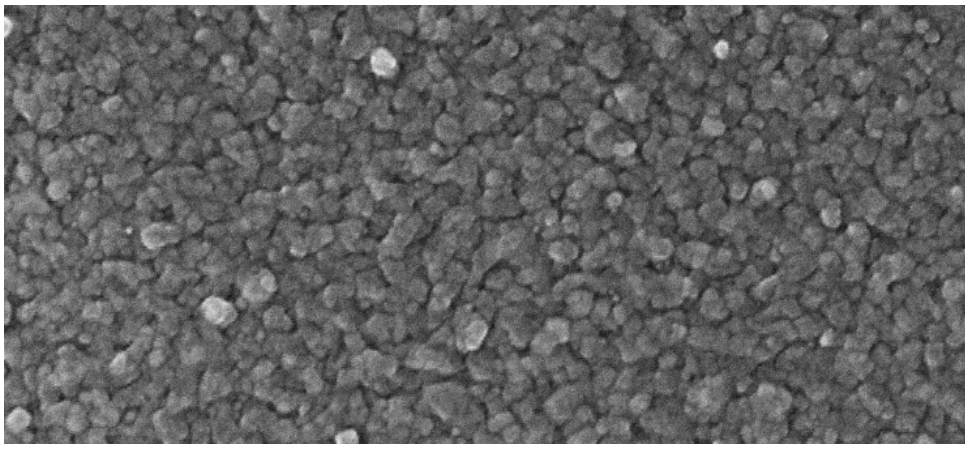

Figure 60: The topview of an Al thin film with big grains.

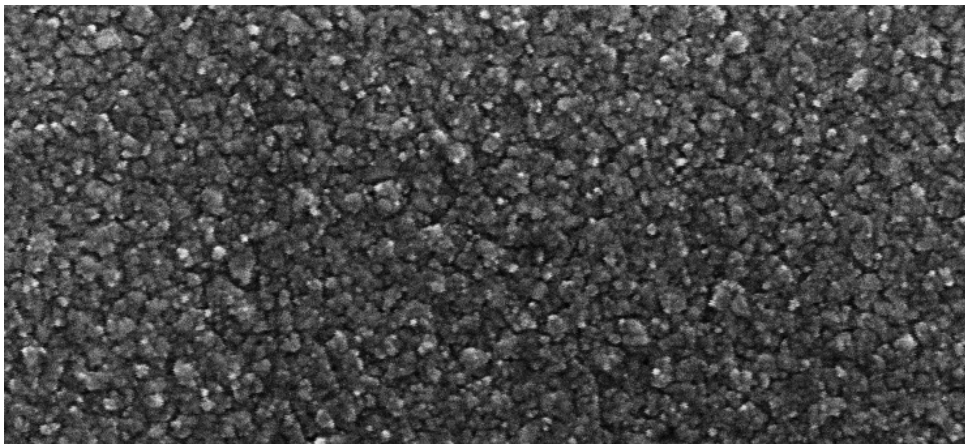

Figure 61: The topview of an Al thin film with small grains.

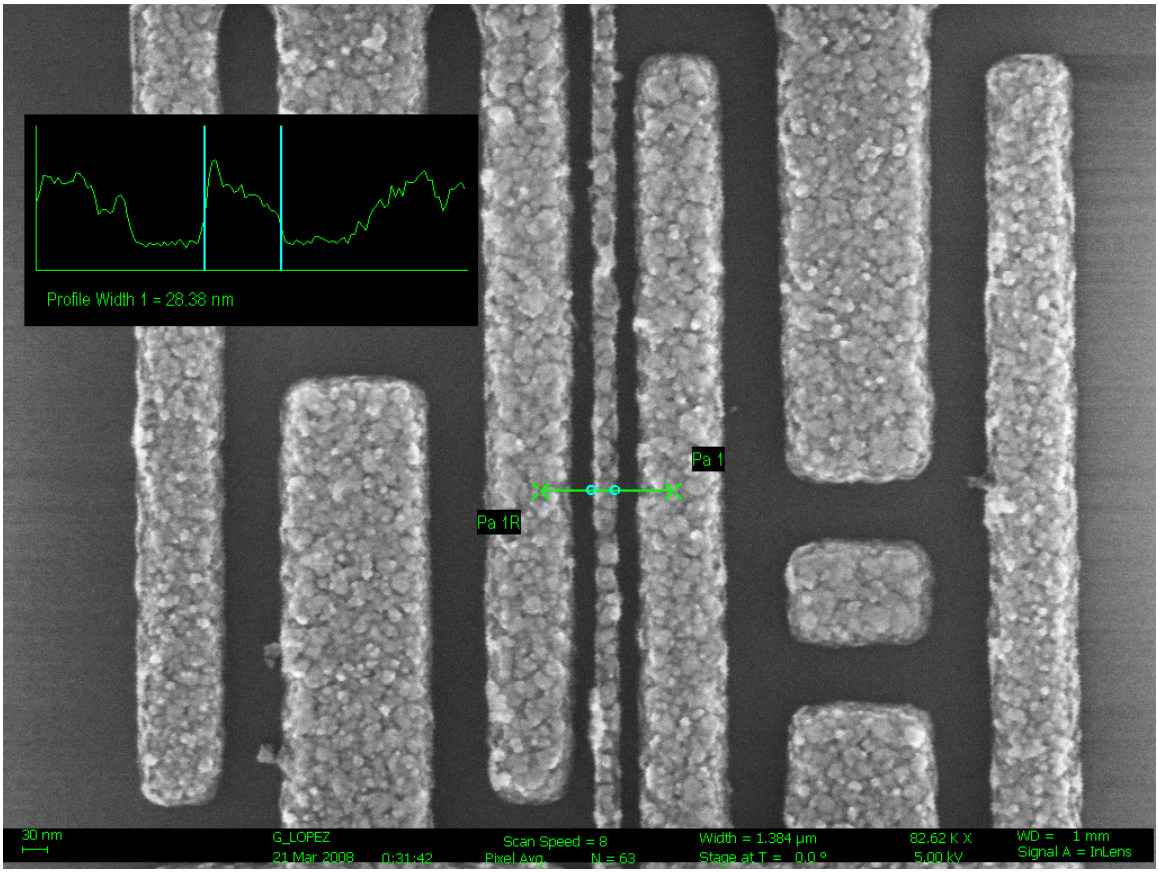

Figure 62: The topview of an Al interconnect with small grains. Smoother surface is evident.

5.5.3.3 Crucible to Sample Line of Sight and Deposition Optimization

To sustain good uniformity across the chip without the use of sample rotation, the line of sight from the crucible to the sample was established (Figure 63). Using two pens attached to a long wire tied with two keys as weights, proper sample mounting was determined to be 2“ from the rear (Figure 64) with the sample centered from left to right as shown in Figure 65. Attention to line of sight allowed for enhanced uniformity across the chip as shown in Al and Cu step height measurements in Table 10 and Table 11, respectively.

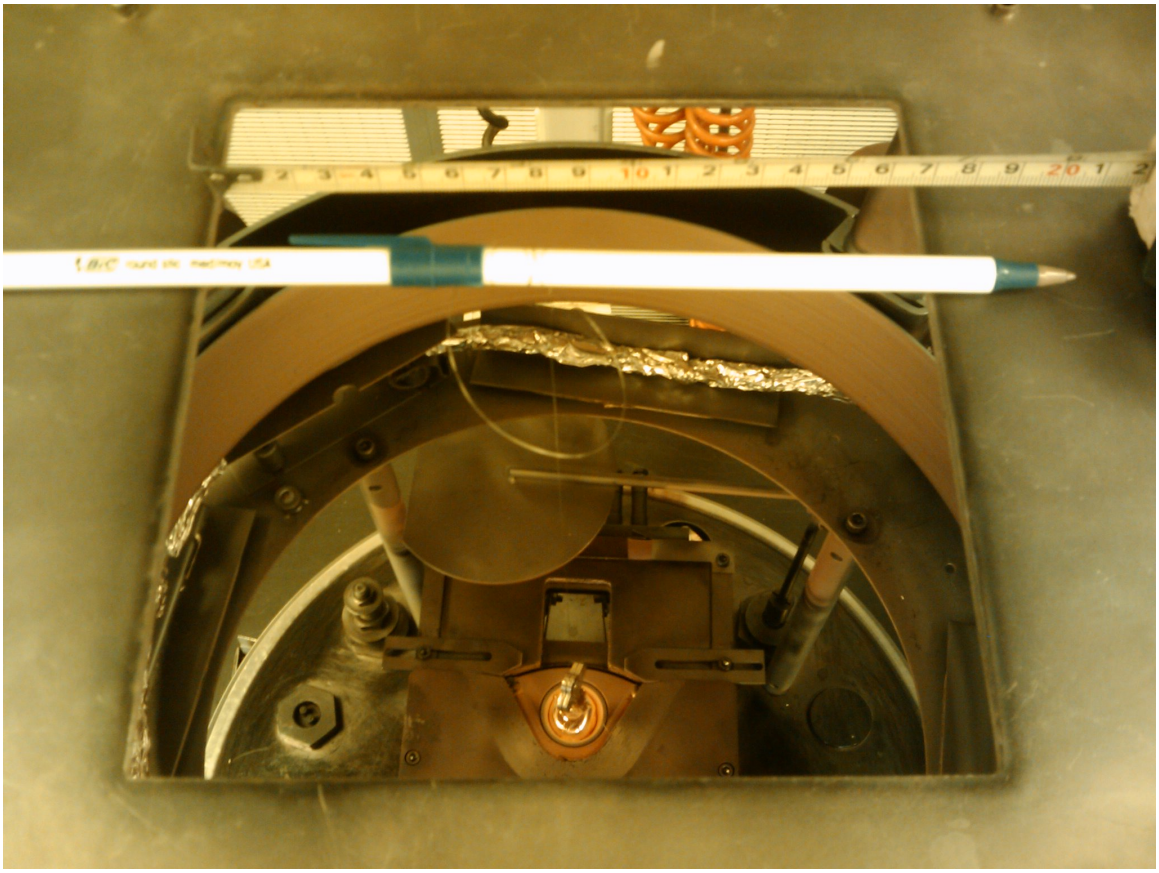

Figure 63: To sustain good uniformity across the chip without the use of sample rotation, the line of sight from the crucible to the sample was determined using two pens attached to a long wire tied with two keys as weights.

Table 10: Sample AFM Aluminum Step Height Measurements

Sample 1	Sample 2
Dialed-In Dep: 120nm @ 0.5Å/s	Dialed-In Dep: 150nm @ 0.5Å/s
32.3	38.9
32.8	39.1
32.6	40.0
32.3	39.6
33.0	38.9
34.5	38.7
	39.8
	38.6
	38.7
Mean: 32.9	Mean: 39.1
$\frac{SD}{Mean} = 2.5\%$	$\frac{SD}{Mean} = 1.3\%$
% Deposited: 27.4%	% Deposited: 26.1%
Chamber Pressure [μTorr]	
Start: 1.5	Start: 1.6
End: 1.4	End: 1.2

Table 11: Sample AFM Copper Step Height Measurements

Sample 1	Sample 2
Dialed-In Dep: 200nm @ 1.0Å/s	Dialed-In Dep: 220nm @ 1.0Å/s
36.3	36.9
37.7	37.9
36.2	40.2
37	38.2
36.9	38.7
37	38.5
37.3	38.8
37.4	39.1
38.7	37.6
38.2	
39.3	
38.6	
38.8	
37.9	
Mean: 37.7	Mean: 38.4
$\frac{SD}{Mean} = 2.5\%$	$\frac{SD}{Mean} = 2.5\%$
% Deposited: 18.8%	% Deposited: 17.5%
Chamber Pressure [μTorr]	
Start: 1.6	Start: 1.8
End: 1.2	End: 1.4

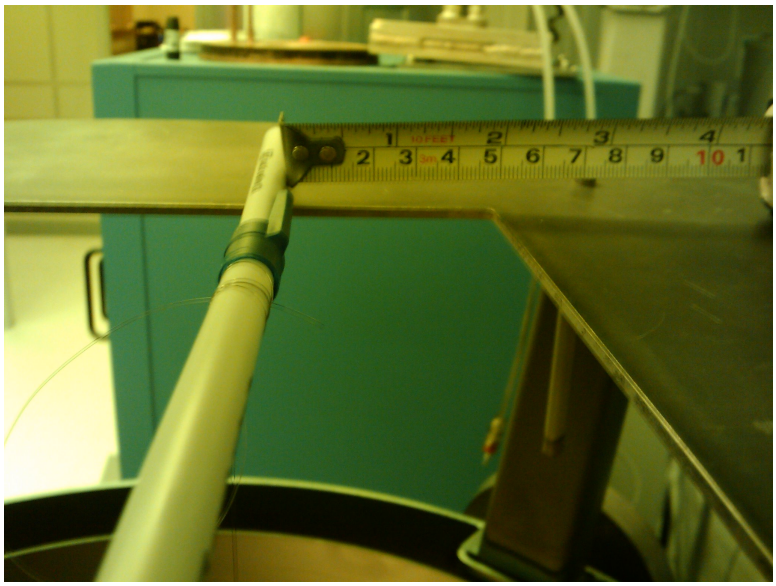

Figure 64: Line of sight from crucible to sample requires the sample be placed 2“ from the rear as shown above and centered left to right.

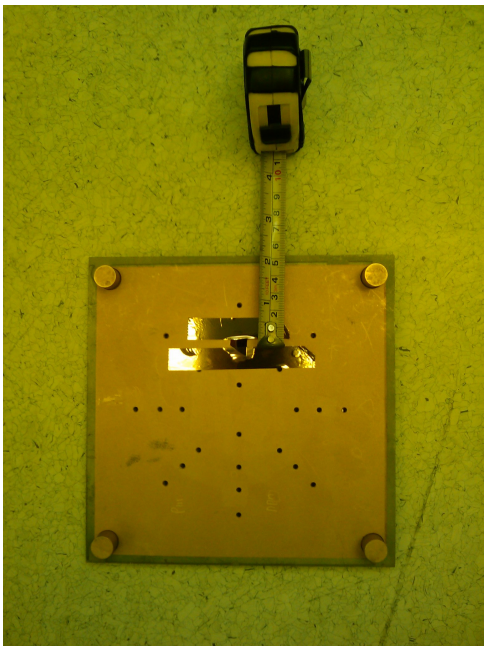

Figure 65: Once the line of sight had been established, a sample undergoing metalization was mounted as shown with kapton tape.

5.6 Conclusions

In order to calibrate the new ρ_{eff} model derived in Chapter 2, interconnects with various linewidths must be fabricated and electrically tested. In this chapter, the fabrication of nanointerconnect test structures was presented. Exhaustive optimization and characterization was required to increase reproducibility, yield and overall quality of the realized structures.

CHAPTER VI

NEW EFFECTIVE RESISTIVITY MODEL CALIBRATION

6.1 Introduction

In Chapter 2, a new physically based ρ_{eff} model was derived. Thus far, the new model has been used to demonstrate the impact of LER, size effects and process variations on interconnect performance using the Fast Interconnect Statistical Simulator engine MIGUEL (Metallic Interconnect Generation Utility for Experimental LER), which was developed in Chapter 4. Using the exhaustively optimized nanofabrication process developed in the previous chapter, metallic interconnect test structures have been fabricated and are used to calibrate the new ρ_{eff} model.

6.2 Fabricated Test Structures

To further validate and calibrate the new ρ_{eff} LER in (82), Cu interconnect test structures (Figure 46) were fabricated with l_{int}=530μm wire lengths. A 1cm^2 Si die with thermally grown 830nm thick SiO_2 was used as the substrate during the fabrication process. A total of 25 interconnect test structures, 5 patterns per wire width, were patterned with varying line-widths. Pattern writing was performed using a JEOL JBX-9300FS E-Beam Lithography tool in 80nm thick polymethyl methacrylate (PMMA) resist with a 1000μC/cm^2 base dose at 2nA with 100kV accelerating voltage. Pattern development submerged the substrate in a solution of 2:1 IPA:H_2O for approximately 15s. Drying followed using N_2. A CVC E-Beam Evaporator deposited a <5nm seed layer of Cr prior to the Cu deposition for adhesion to the SiO_2 surface. Metal lift-off was then performed using a bath of Shipley Microposit Remover 1165 at 85°C followed by a bath and rinse of isopropyl alcohol (IPA).

Similarly, Al interconnects were fabricated but with l_{int}=5μm wire lengths using the

configuration shown in Figure 45. A total of 35 Al interconnect test structures were patterned with varying line-widths. A direct AMI rinse was applied to the chip after soaking in a bath 1165 at 85°C for 10min.

6.3 Metrology

In order to calibrate the new ρ_{eff} model in (82), physical and electrical data must be obtained from the realized test structures. Physical metrology is performed using the Carl Zeiss SEM for top-view lateral measurement, while the Veeco Atomic Force Microscope is used to measure step height of the thin film.

6.3.1 Physical Measurement

Physical metrology is performed using a Veeco AFM and a Carl Zeiss Ultra 60 SEM. The AFM determined that the wire thickness, h_0 was consistently 48nm across the fabricated Cu lines. Using the SEM, w_0 was determined by taking sample averages of w' and w'' (Figure 16). Average values for w', w'', w_0, and LER for each drawn CD are found in Table 12. An SEM graph of a fabricated Cu interconnect with LER is shown in Figure 46. Effective line widths were calculated to be 332nm, 229nm, 93nm, 75nm, and 61nm. Total average on-chip LER was determined to be 14nm.

Table 12: SEM Cu Line Width Measurement Averages

w' [nm]	w'' [nm]	w_0[nm]	LER [nm]
317	348	332	16
217	242	229	13
77	110	93	16
63	87	75	12
47	76	61	14
Total Average On-Chip LER [nm]			14

A total of 35 Al interconnect test structures with h_0=39nm were fabricated with w_0's of 50nm, 53nm, 56nm, 59nm, 73nm, 74nm and 83nm. Total average LER was determined to be 7nm. An SEM graph of a fabricated Al interconnect is shown in Figure 45. Average values for w', w'', w_0, and LER for each drawn CD are found in Table 12.

Table 13: SEM Al Line Width Measurement Averages

w' [nm]	w'' [nm]	w_0 [nm]	LER [nm]
42	58	50	8
48	59	53	5
51	61	56	5
53	66	59	7
63	82	73	9
65	82	74	9
75	91	83	8
Total Average On-Chip LER [nm]			7

6.3.2 Electrical Measurement

Electrical measurements are performed using the Hewlett Packard 4156A Precision Semiconductor Parameter Analyzer in a 2-point probe configuration. Copper contact resistance was less than 5Ω at 1V and was negligible compared to the measured resistances that were 3-4 orders of magnitude higher. Of the 25 Cu wires that were fabricated, only 20 were testable. Each testable wire was measured twice, yielding an average resistance. Values are tabulated in Table 14 The effective resistivity of the test wires was estimated using the expression

$$\rho_{eff} = \frac{R_{int} \times w_0 \times h_0}{l_{int}}. \tag{105}$$

Table 14: Extracted R_{int} at 1.0V and calculated ρ_{eff} grouped by w_0 for 530μm Cu wires

332nm		229nm		93nm		75nm		61nm	
kΩ	$\mu\Omega$-cm	kΩ	$\mu\Omega$-cm	kΩ	$\mu\Omega$-cm	kΩ	$\mu\Omega$-cm	kΩ	$\mu\Omega$-cm
1.41	4.44	2.14	4.76	6.21	6.43	9.04	7.79	12.28	9.36
1.43	4.50	2.15	4.77	6.21	6.42	8.95	7.72	12.16	9.27
1.44	4.50	2.14	4.76	6.25	6.47	8.93	7.70	12.22	9.32
1.44	4.53			6.28	6.50	9.08	7.83		
1.43	4.52					9.03	7.79		

Aluminum contact resistance was ∼20Ω at 1V. Of the 35 Al wires that were fabricated, only 26 were testable. Each testable wire was measured yielding a resistance value with a corresponding computed ρ_{eff} using (105). The resistance and ρ_{eff} values are tabulated in Tables 15 and 16. In Figure 66, ρ_{eff} values are plotted against w_0. Effective resistivity values are extremely high possibly due to the self-passivation of the aluminum, which forms aluminum oxide. As a result of the significantly higher values compared to the Cu measurements in Table 14, it is determined that while the models may show significant performance improvement with Al and its short electron mean free path, practically, the metal is limited by its affinity to react with its environment as also discussed in [5, 6].

Table 15: Extracted R_{int} at 1.0V and calculated ρ_{eff} grouped by w_0 for 5μm Al wires

50nm		53nm		56nm		59nm	
kΩ	$\mu\Omega$-cm	kΩ	$\mu\Omega$-cm	kΩ	$\mu\Omega$-cm	kΩ	$\mu\Omega$-cm
1.75	69.0	1.58	66.3	1.37	60.6	1.17	54.5
1.89	73.9	1.48	62.1	1.35	59.4	1.16	53.8
1.81	71.0	1.51	63.2	1.34	59.2	1.17	54.4
						1.12	52.2

Table 16: Extracted R_{int} at 1.0V and calculated ρ_{eff} grouped by $w_0$for Al

73nm		74nm		83nm	
kΩ	$\mu\Omega$-cm	kΩ	$\mu\Omega$-cm	kΩ	$\mu\Omega$-cm
0.93	53.2	0.88	50.9	0.75	49.0
0.92	52.4	0.85	49.2	0.76	49.8
0.86	48.7	0.85	49.0	0.75	48.6
0.88	50.1	0.80	46.2	0.69	45.2
		0.76	43.7		

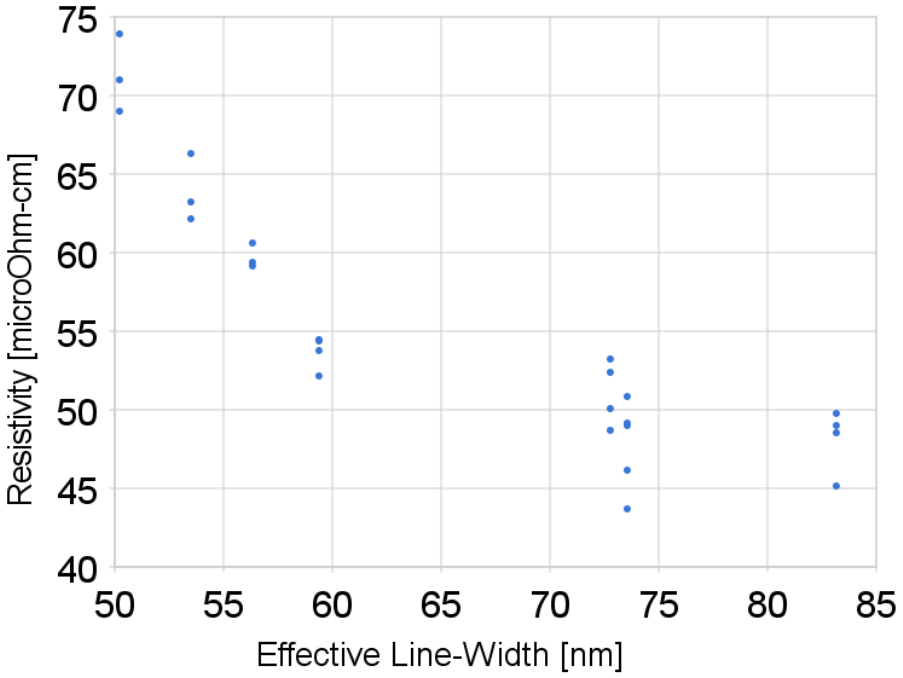

Figure 66: Al interconnect effective resistivity vs. effective line-widths. Values for effective resistivity were found to be substantially higher than the values reported in [5] and [6]. This is most likely due to the self-passivation (oxidation) of Al and the interaction of the alumina with the electrons when under test.

6.4 Effective Resistivity Model Calibration

Using equation (105), where R_{int} is the average wire resistance and l_{int} is the wire length of 530μm, twenty Cu ρ_{eff} values were extracted and plotted in Figure 67. Table 14 lists the actual resistance measurements and calculated ρ_{eff}values. Calibration of (82) to the plotted data in Figure 67 required numerical analysis using ROSE. ROSE statistically determines the best fit for a range of p and R with a predetermined LER value. The value of p can be between 0 and 1, where a value of 0 indicates scattering is totally diffuse (inelastic) with the electrons experiencing complete loss of their drift velocity. In other words, p indicates the percentage of electrons that are to be scattered elastically at the surface of the thin film and losing no energy. The scattering parameter R indicates the percentage of electrons that are scattered at the grain boundary and has a value between 0 and 1. For R=1, an electron will experience complete internal reflection within a metallic grain. To best fit the LER model to the experimental data, the values of p=0 and R=0.79 for 14nm LER were found. The resulting LER model is plotted in Figure 67 and agrees well with the data. For comparison, the FS-MS model with p=0 and R=0.79 is also graphed in Figure 67. As expected, the traditional FS-MS model underestimates the value of the ρ_{eff} where LER effects begin to become more pronounced.

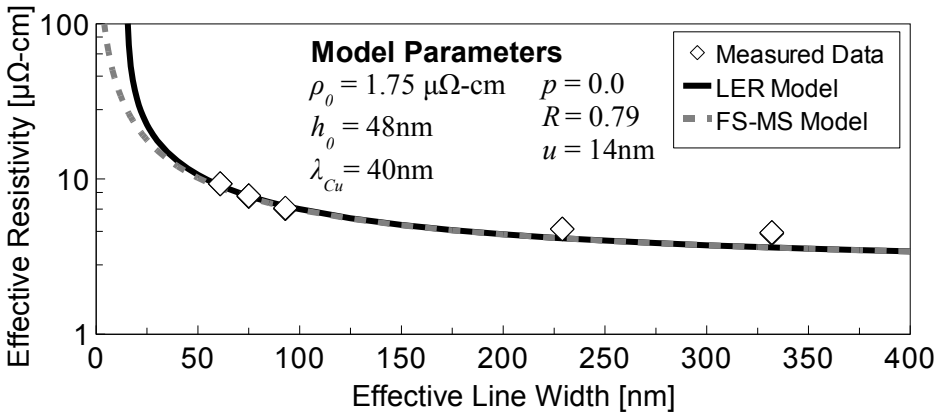

Figure 67: Comparison of resistivity model projections from (6) and (82) with electrical measurements of fabricated test structures with 61-332nm line widths. The model in (82) is a function of LER, p and R. Average grain size d is considered to be equal to w_0 [3, 15]. The value of ρ_0 is obtained from [15].

6.5 Conclusions

The measurement of both Al and Cu nano-interconnect test structures have been performed. Due to aluminum's affinity to self-passivate, ρ_{eff} values were extremely high, resulting in the lack of a model fit. Model calibration did occur using empirical data from fabricated copper test structures. Using ROSE, calibration revealed the scattering parameters of p=0.0 and R=0.79 to best fit the data to the model in (82) with an average LER of 14nm. More importantly, the traditional FS-MS model is shown to underestimate the value of the ρ_{eff} where LER effects begin to become more pronounced.

CHAPTER VII

CONCLUSIONS AND FUTURE WORK

7.1 Introduction

Scaling copper interconnects at the 22nm technology node are problematic because size effects become pronounced as critical dimensions approach the electron mean free of copper (λ_{Cu}=40nm). In this work, five tasks, each with a unique contribution, have been completed. In these tasks, the impact of size effects, line-edge roughness and process variations on the effective resistivity of the copper interconnect has been demonstrated through modeling, simulation and experimentation.

7.2 Task I: The New Effective Resistivity Model Derivation

Task I involved the derivation of a new physical model for effective resistivity as a function of line-edge roughness and size effects. Sensitivity to LER and the selection of scattering parameter values was demonstrated using ITRS 2007 ρ_{eff} target values. The analysis revealed that while certain scattering parameters values can be chosen to best fit ρ_{eff} data, when LER is introduced, effective resistivity is exacerbated especially as $p \rightarrow 0$.

7.3 Task II: Critical Path Model Enhancement

Task II enhanced a former critical path model by the inclusion of interconnect RC parasitics, where the previous model only considered interconnect capacitance. This task involved the survey of foundry data to estimate device resistance for use in a Monte Carlo statistical simulator in Task III. Using the new CP model, the benefit of a short-wire architecture such as a multi-core design was demonstrated. Moreover, a case study on the 11nm node elucidated the important trade-off between core complexity and clock frequency. It noted that if LER and size-effects are ignored in local CP models, MPU design windows could be completely off the desired frequency targets.

7.4 Task III: The Fast Interconnect Statistical Simulator (FISS)

Task III enabled the Fast Interconnect Statistical Simulator (FISS), which is comprised of two statistical engines: the Regression Optimizer for Size Effects (ROSE) and the Metallic Interconnect Generation Utility for Experimental LER (MIGUEL). ROSE facilitates parameter extraction (eg. p and R) for the new ρ_{eff} model in Task I. MIGUEL allows the evaluation of single and multi-core MPU Maximum Critical Path Delays corresponding to each of the ITRS technology generations. In addition to a short-wire architecture such as a multi-core system, simulations using MIGUEL indicated that using a material with a $\lambda<\lambda_{Cu}$ may offer an increased tolerance to size effects that manifest at the sub-40nm line-width for Cu.

7.5 Task IV: Nano-Metallic Interconnect Test Structure Fabrication

Task IV optimized and fabricated interconnect test structures in aluminum and copper with minimum line-widths of 50nm. Nano-enabled tools such as the JEOL E-Beam Lithography machine, CVC E-Beam 1 Evaporator, Carl Zeiss SEM and Veeco AFM were needed to facilitate this task. A minimum line-width of 20nm with a length of 10μm was fabricated as a part of this research. Its integrity as a wire was verified with the Carl Zeiss SEM, but electrical testing was not possible due to pad integration issues (eg. backscattering).

7.6 Task V: The New Effective Resistivity Model Calibration

Finally, using the fabricated test structures from Task IV, Task V completed the experimental portion of this work. The calibration of the model in Task I to empirical data demonstrated the limitation of the former FSMS model especially when the LER becomes a significant percentage of the effective line-width. In short, the body of this dissertation has come full circle from model derivation to model simulation/system-level analysis to experimental calibration.

7.7 Future Work: Graphene

While target values are open to change in the ITRS, the integration of a novel material tolerant to size effects and, ultimately, scaling is needed to replace the copper interconnect. Today one such material is being explored; that material is graphene. As a mono-atomic layer of carbon, the intrinsic ballistic transport properties of graphene has the ability to exceed the projected performance of copper at the end of the roadmap [143]. Additionally, graphene may also have the ability to replace the transistor as demonstrated by [144]. In the end, the hurdle of integration and innovation for the next generation of nano-electronics exists, and its evolution will be limited only to the imagination and ingenuity of its creators.

APPENDIX A

LIST OF PUBLICATIONS AND PRESENTATIONS

1. G. Lopez, J. Davis, and J. Meindl, "A new physical model and experimental measurements of copper interconnect resistivity considering size effects and line-edge roughness (LER)," in Proceedings of the IEEE 2009 International Interconnect Technology Conference, 1-3 June 2009. Sapporo, Japan: IEEE, 2009.

2. A. J. Joshi, G. G. Lopez, J. A. Davis, "Design and optimization of on-chip interconnects using wave-pipelined multiplexed routing," IEEE Transactions on Very Large Scale Integration Systems, Volume 15, Issue 9, pp. 990 1002, Sept. 2007.

3. G. Lopez, R. Murali, R. Sarvari, K. Bowman, J. Davis, and J. Meindl, "The impact of size effects and copper interconnect process variations on the maximum critical path delay of single and multi-core microprocessors," in Proceedings of the IEEE 2007 International Interconnect Technology Conference, 4-6 June 2007. Burlingame, CA, USA: IEEE, 2007.

4. G. G. Lopez, G. Fiorenza, T. Bucelot, P. Restle, M.Y. Lanzerotti. "Characterization of the impact of interconnect design on the capacitive load driven by a global clock distribution," Great Lakes Symposium on VLSI, April 2005.

5. Poster: G. G. Lopez, G. Fiorenza, T. Bucelot, P. Restle, M.Y. Lanzerotti. "Circuit and wire contributions to clock power in IBM server group microprocessor designs," Austin Conference on Energy-Efficient Design, March 2004.

APPENDIX B

FISS USER GUIDE

B.1 Introduction

The Fast Interconnect Statistical Simulator houses two multi-threaded statistical engines for interconnect resistivity analysis as explained in greater detail in Chapter 4. This manual simply provides screenshots as a preview/overview to navigating and using the software. Requests to view and use this software can be sent to geraldlopez@gmail.com.

B.2 Registration and Login

In order to login and use FISS, one must register with the site. You may register with the site by clicking *Register for a new account* found on the login page as show in Figure 68.

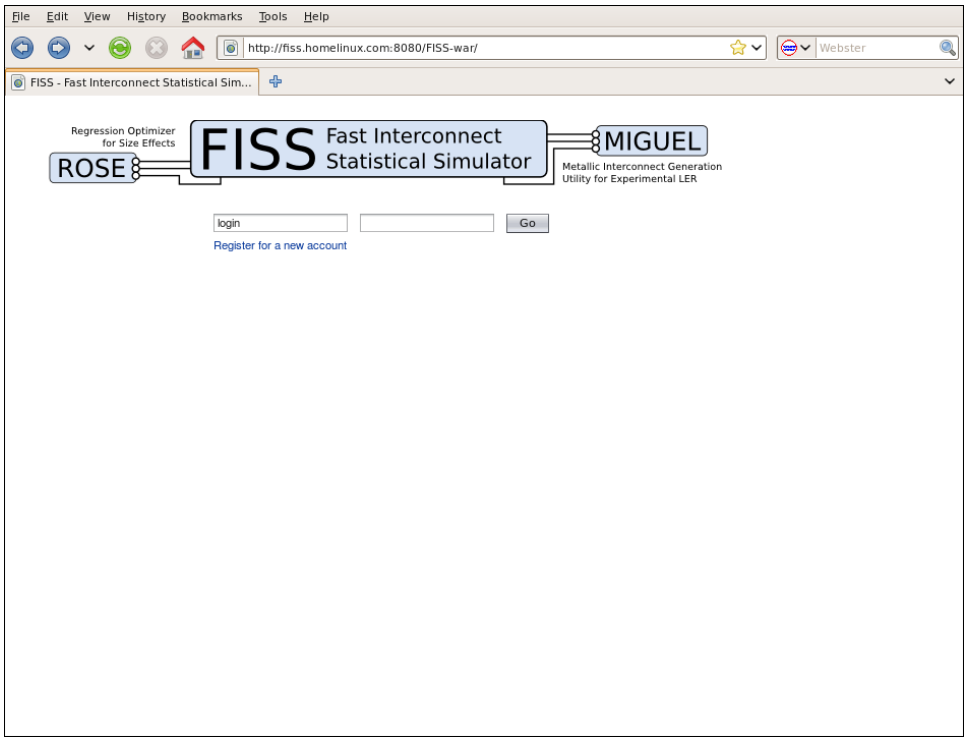

Figure 68: The Fast Interconnect Statistical Simulator login page

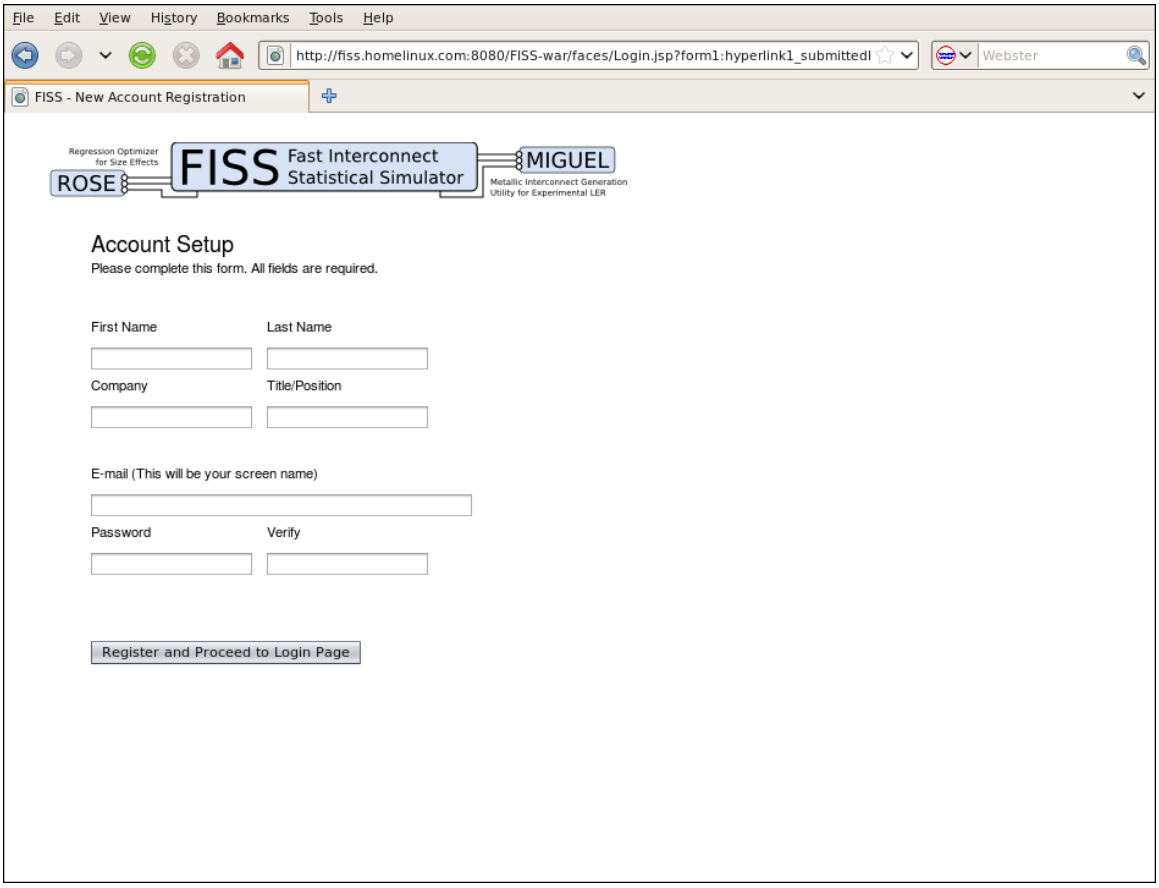

Figure 69: The Fast Interconnect Statistical Simulator registration page

On the registration page, you must enter all fields and click *Register and Proceed to Login Page* button, where you will be sent back to the login page as shown in Figure 68. On the login page, simply enter your login and password with which you registered and click *Go*. If successful, you will sent to the FISS dashboard as shown in Figure 70.

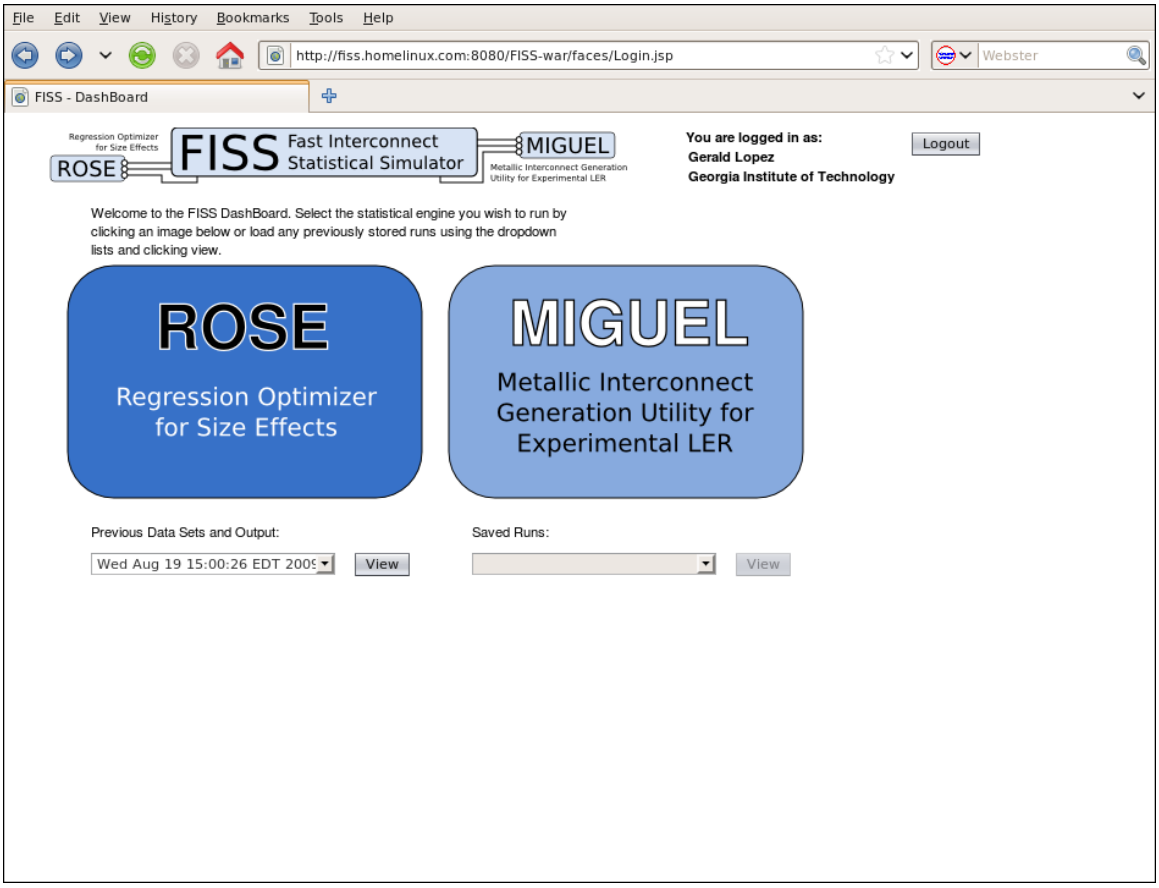

Figure 70: The Fast Interconnect Statistical Simulator Dashboard

In the FISS dashboard as shown above in Figure 70, you will be able to select one of the two statistical engines within the software. By clicking on the ROSE graphic, you will be entered into the ROSE interface to execute regression optimization using the new ρ_{eff} model in (82). By clicking on the MIGUEL graphic, you will be entered into the MIGUEL interface to execute circuit/system level analysis for the maximum critical path delay of future ITRS technology nodes using the new ρ_{eff} model in (82) for single core and multi-core architectures. Previous results of ROSE and MIGUEL are made available by date in the dropdown box under the corresponding graphics on the dashboard. Selecting the date and clicking the *View* button will display results of stored runs.

B.3 ROSE: Regression Optimizer for Size Effects

If you clicked on the ROSE graphic on the FISS dashboard in Figure 70, you should be now viewing the ROSE interface (Figure 71) for which to execute regression optimization using experimental data. By default, ITRS 2007 parameters are entered in the *Effective Resistivity Measurements* text box with effective bulk resistivity of 2.2$\mu\Omega$-cm and a mean free path of 40nm for Cu. Tests for different values of LER may be performed. By default 4 different values of LER are entered and selected for testing. At least one LER must be tested and is guaranteed as a failsafe. Once all desired parameters are entered, click the *Perform Regression Optimization* button to execute the ROSE engine.

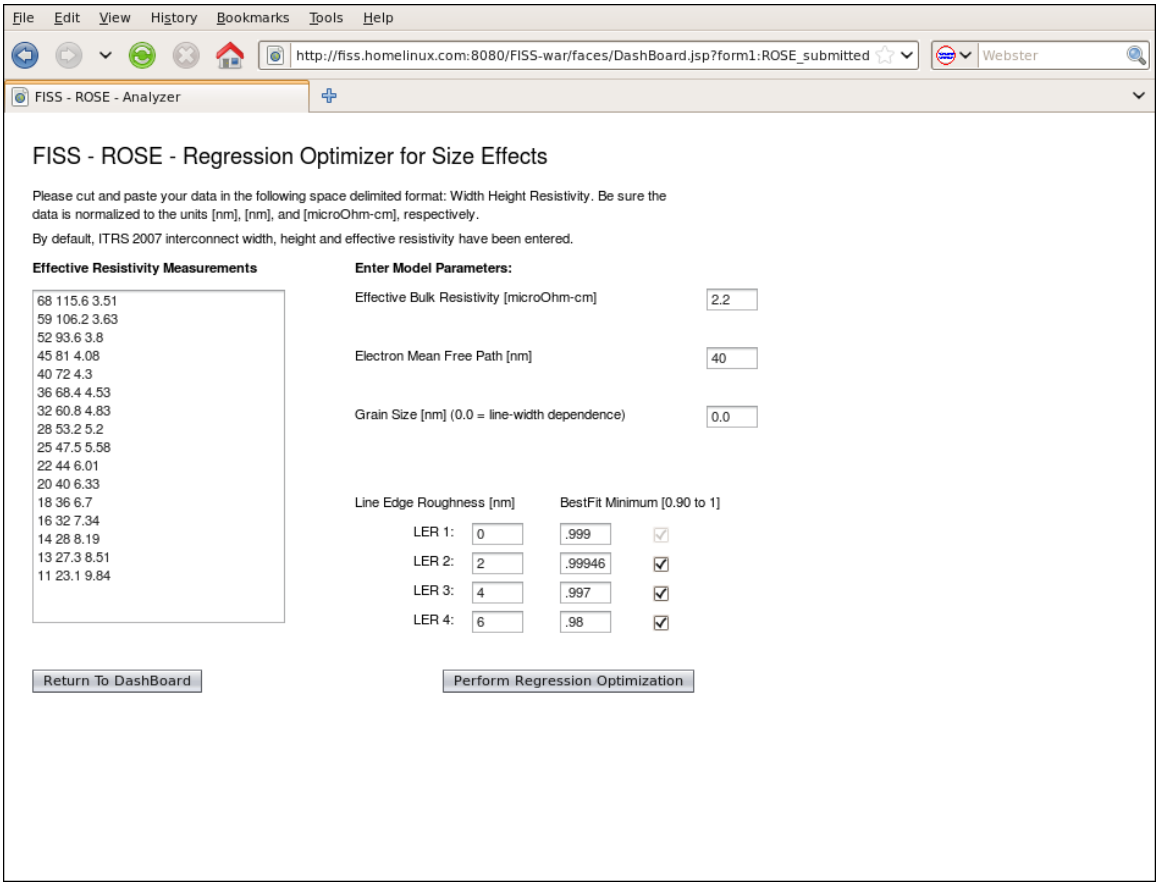

Figure 71: The Fast Interconnect Statistical Simulator Regression Optimizer for Size Effects (ROSE)

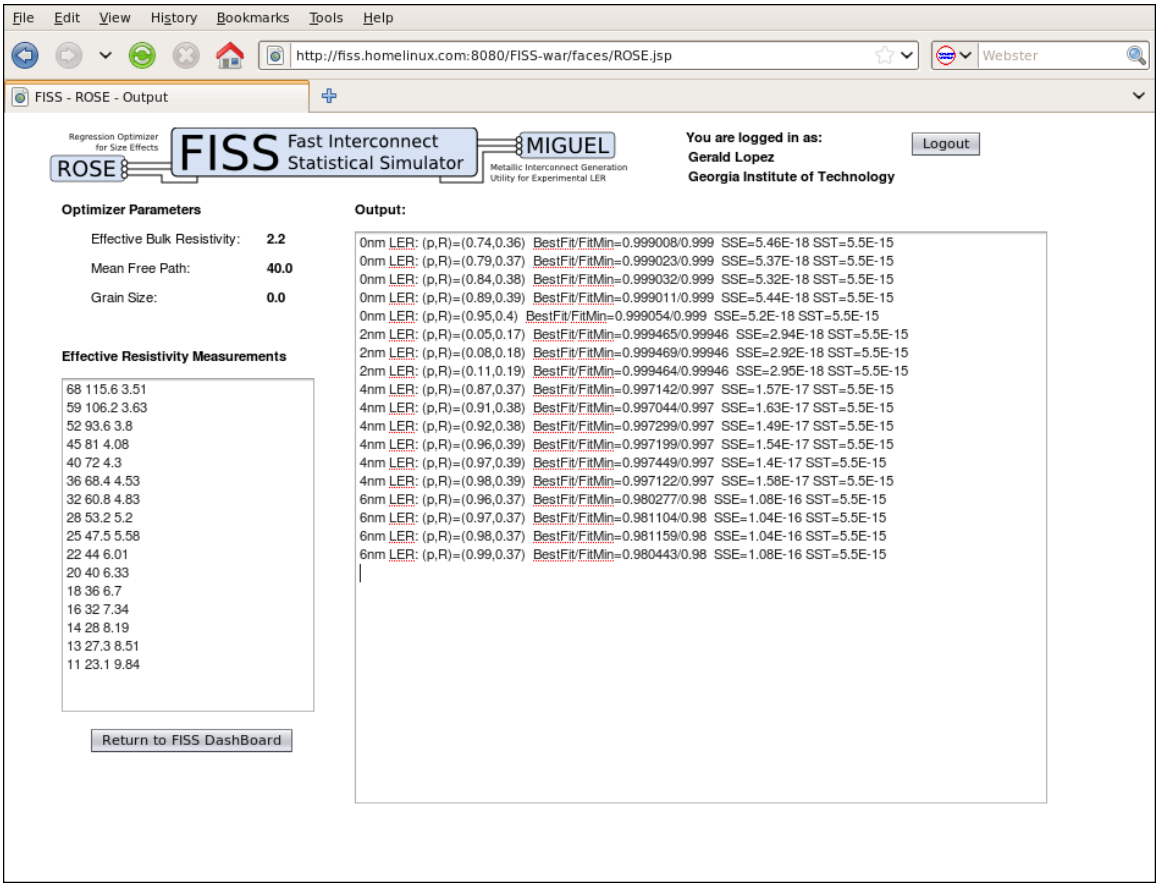

Figure 72: The Fast Interconnect Statistical Simulator ROSE output page

If the ROSE engine is executed with the default ITRS 2007 parameters, a screen similar to Figure 72 above with output should appear. This information is automatically stored in the database for later retrieval. Currently, there is no way to delete stored runs from the database.

B.4 MIGUEL: Metallic Interconnect Generation Utility for Experimental LER

If the MIGUEL graphic on the FISS dashboard in Figure 70 is clicked, the MIGUEL interface (Figure 73) for which to execute the maximum critical path delay for each ITRS technology node will be rendered. By default, specularity and reflectivity is set to p=0.0 and R=0.5, respectively. Tests for different values of LER may be performed in addition to specific technology nodes. At least one LER must be tested. The first LER parameter is selected as a failsafe. Once all desired parameters are entered, click the *Run Simulations* button to execute the MIGUEL engine.

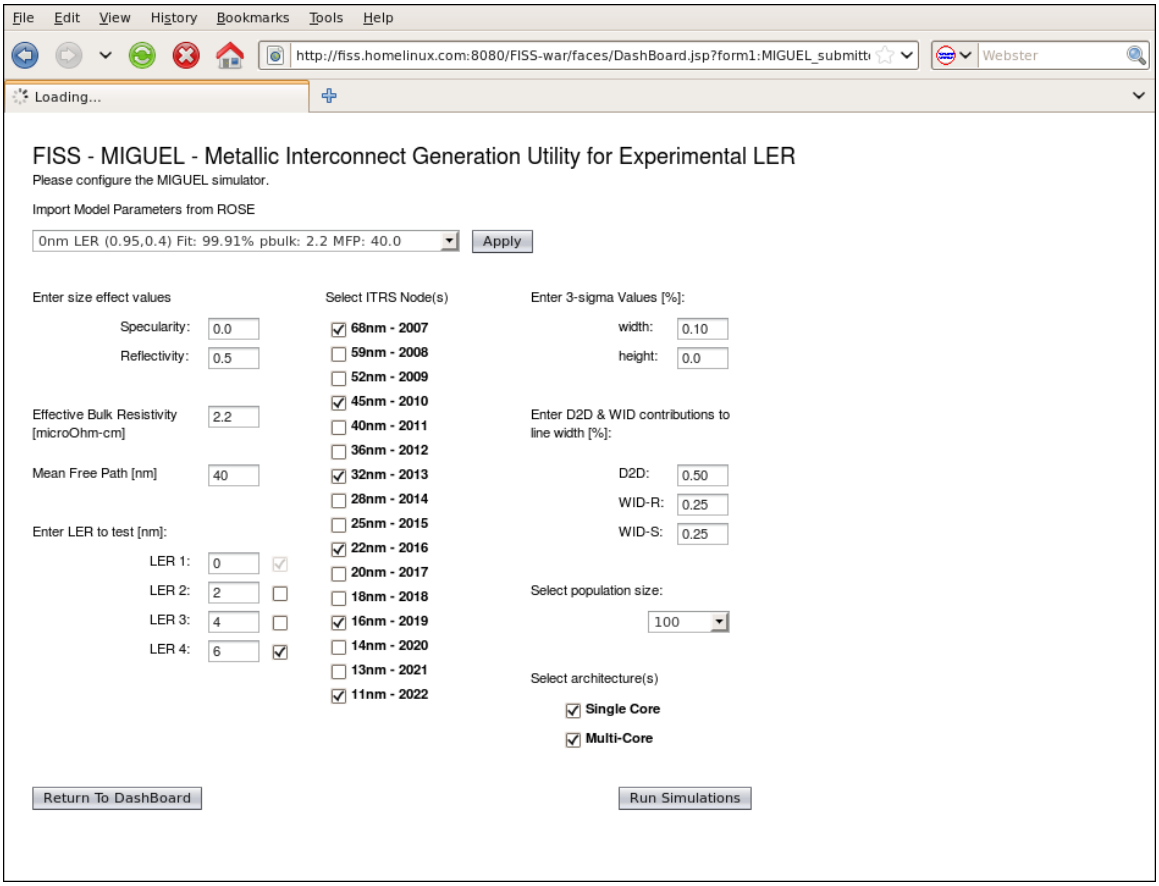

Figure 73: The Fast Interconnect Statistical Simulator Metallic Interconnect Generation Utility for Experimental LER (MIGUEL)

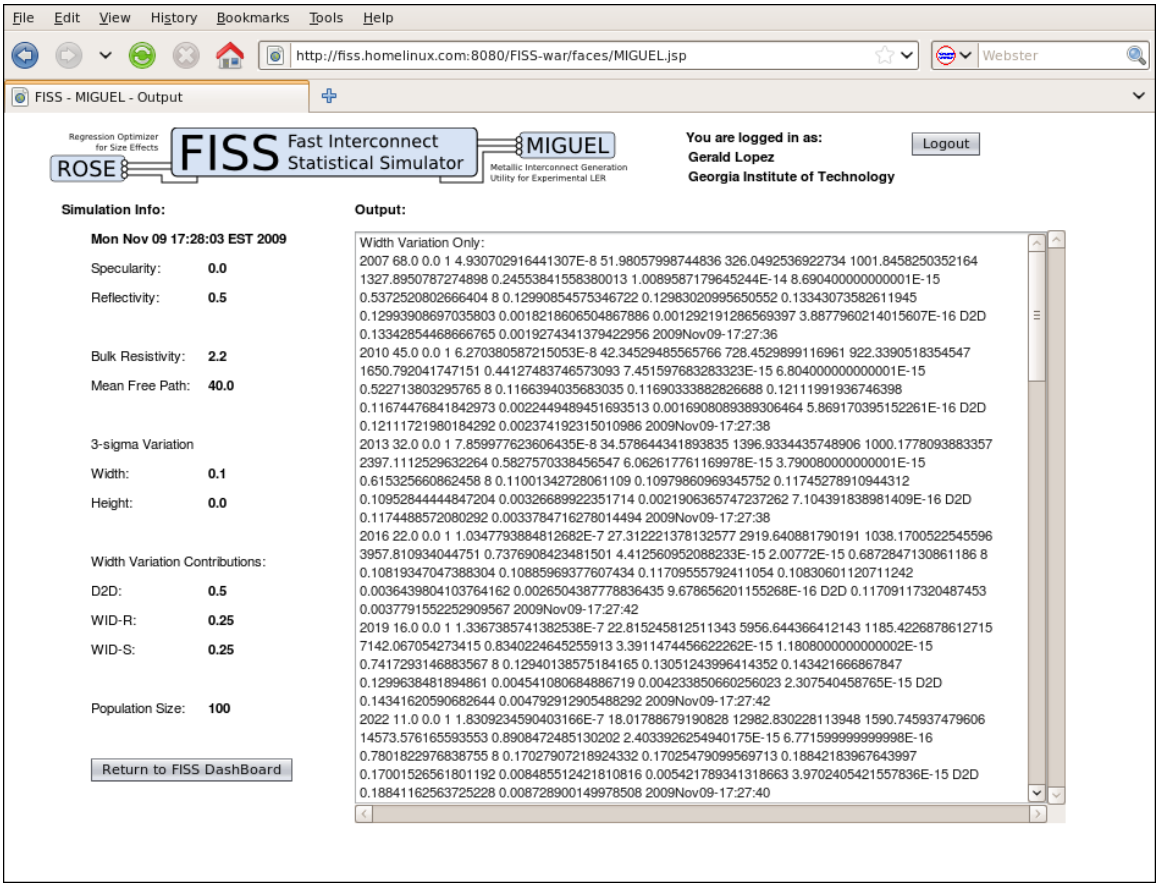

Figure 74: The Fast Interconnect Statistical Simulator MIGUEL output page

If the MIGUEL engine is executed with the desired parameters, a screen similar to Figure 74 above with output should appear. This information is automatically stored in the database for later retrieval. Currently, there is no way to delete stored runs from the database.

APPENDIX C

THE IITC 2009 EXAMPLE

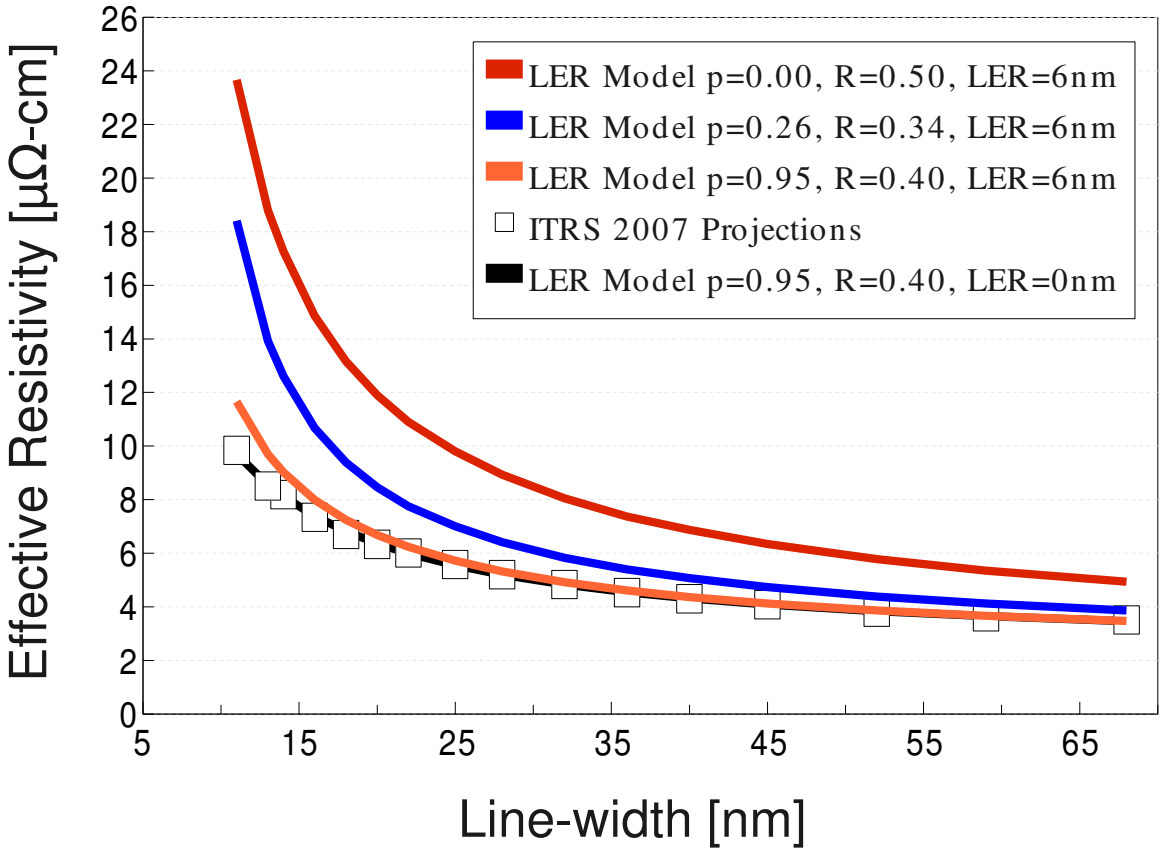

Figure 75: The example graph first presented at the IITC 2009 in Sapporo, Japan demonstrating the importance of the new ρ_{eff} model in (82) and its sensitivity to the values of p, R and LER.

The graph in Figure 75 was never officially published in the 2009 International Interconnect Technology Conference (IITC) paper [50]. It was presented in the oral presentation as it best demonstrates the importance of the new ρ_{eff} model in (82) and its sensitivity to the values of p, R and LER. The solid black line represents the ITRS 2009 projections for copper ρ_{eff} with p=0.95 and R=0.40 with 0nm of LER. By adding 6nm of LER, the solid orange line increases ρ_{eff} for the 11nm node by 20%. However, the model in (82) demonstrates

further sensitivity to size effects when they are adjusted to average values found in Table 2, where p=0.26 and R=0.34 with 6nm of LER in the solid blue line. The result increases the ρ_{eff} by 87% when compared to ITRS 2007 11nm node projection. Finally, the solid red line increases the 11nm node ρ_{eff} projection by 140%, when scattering parameters are adjusted to p=0.00 and R=0.50 with 6nm of LER.

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VITA

Gerald G. Lopez graduated as valedictorian from Southern High School in Harwood, Maryland in May 1997. As Cum Laude, he received his Bachelor of Science in Computer Engineering in December 2001, from the University of Maryland, Baltimore County as a Meyerhoff Scholar (M9). He received his Master of Science in Electrical and Computer Engineering and a Doctorate of Philosophy in Electrical and Computer Engineering in July 2004 and December 2009, respectively, from the Georgia Institute of Technology in Atlanta, Georgia.